Checklist for EE143 Final Exam Fall 2010

Overview of silicon processing modules, process sequence, and device structures
Qualitative understanding of all processing modules .
Typical temperature range of all process modules.
Concept of a Process Flow and simple examples. Patterning, masking layers, sacrificial layers. Make sure the processing temperature is lower than degradation temperature of materials already present on the structure.
How to read Top view and Cross-sectional view of simple structures and devices.

Silicon electrical properties
Electrons and Holes. Dopants (donors and acceptors). Mobility. Electrical Resistivity. Sheet resistance.

Lithography
Contact printing, Proximity Printing, Projection Printing
Overlay errors – thermal run-in/run-out, translational error, rotational error
Minimum resolution and depth of focus calculations
Resist – positive and negative resist mechanism (qualitative), resist contrast
Conceptual understanding of Aerial image formation, Image Contrast. Standing Wave effect, Phase Shift Mask, Immersion Lithography, Double Patterning, Proximity scattering, X-ray lithography, E-Beam Lithography.

Thermal Oxidation
Volume change caused by thermal oxidation of Si
Deal-Grove Model for Oxidation
Calculation of oxide grown using: (1) B and B/A constants and (2) oxidation charts
Oxidation rates : Effects of Oxidant (O2 and H2), Si crystal orientation, Pressure, Substrate Dopant Concentration, and Addition of HCl .
Local Oxidation (LOCOS) Process Sequence
Dopant redistribution during oxidation (***qualitative only***)

Ion Implantation
Qualitative understanding of Energy Loss Mechanisms & Substrate Damage
Gaussian approximation of implantation profile. Projected Range (Rp) and Longitudinal Straggle(ΔR_p).
Relationships of dose, beam current, implantation time, implant area, and concentration.
Calculation of sheet resistance and junction depths.
Two-dimensional Implantation profile, Transverse Straggle (ΔR_t) -qualitative
Ion Channeling (qualitative)
Transmitted Fraction through finite mask thickness

Dopant Diffusion
Diffusion Mechanisms, point defects (qualitative)
Characteristics of Predeposition and Drive-in steps

Diffusion Constant and its temperature dependence
Constant-D Diffusion Equation and solutions:
Predeposition $\rightarrow$ erfc function, Drive-in $\rightarrow$ half-gaussian function
Diffusion Profile of Gaussian Implantation.["Method of images" not required in exam]
Calculation of Junctions Depth.
Irvin's Curves - Establish relationship between C_0, x_j, R_S, N_B
2-Dimensional Diffusion Effects. Lateral junction depth under mask yj ~ 0.7-0.8x_j
High Concentration Diffusion Effect (**qualitative** understanding) - E-field Enhancement and Charged Point Defects Enhancement
Oxidation Enhanced Diffusion and Transient Enhanced Diffusion (**qualitative** only)

Thin Film Deposition
Vacuum basics , Pumps and plasma generation (qualitative).
Evaporation Deposition ,Sputtering Deposition, and Chemical Vapor Deposition (mass – transport limited versus surface reaction limited mechanisms)
Thickness non-uniformity calculations
Step coverage problems and deposited thin film cross-sections on nonplanar surfaces
CVD growth rate (Grove Model) and dependence on pressure , temperature, and gas flow rate. Mass depletion issues.
PECVD, ALD (qualitative)

Etching

Etch Bias, Degree of Anisotropy, Etching selectivity
Cross-sections of etching profiles
Worst case design considerations
Wet etching mechanism and examples (qualitative)
Anisotropic wet etching (KOH and EDP)
Reactive Ion Etching mechanisms (qualitative)
How to control Degree of Anisotropy and Etching Selectivity of RIE

Metallization

Simple calculations of RC Time Delay, Interconnect resistance, Contact resistance
Problems with Al as metallization material – Al Spiking and Electromigration
Qualitative understanding of why Cu, W, diffusion barrier, and low-k dielectrcis are used.
Surface Planarization Techniques (qualitative) – SOG, Etch-back, and CMP

Process Integration
Self-aligned structures- channel stop, source/drain, LDD, and SALICIDE
Generic NMOS process flow example
Generic CMOS process flow example – the MOSIS process
Miscellaneous special examples – retrograde well, Gate-Last process, SOI (qualitative)
Given an IC structure, design a process flow

Layout Design Rules
Generate layouts using the simple set of EE143 design rules
Qualitative reasoning of how design rules can be changed if device structure changes

MOS Devices
Accumulation mode, Depletion mode , and Inversion mode of a MOS device
Relationship of V_T to gate material, substrate doping type, substrate doping concentration, gate oxide thickness, channel-body bias, substrate bias, threshold implant, and oxide charges.
Short channel and narrow width effects (qualitative)
I-V characteristics of MOSFET and device parameter extraction
Small-Signal Capacitance versus V_G and device parameter extraction

MEMS
Stress, Strain, Young's Modulus, Poisson Ratio, Yield Stress
Effect of thin-film stress (intrinsic, thermal expansion, external) on cantilever curvatures (qualitative)
Substrate warpage calculations – Stoney's Equation
Stiction problems and solutions
Bonding and Molding (qualitative)
Principle of MEMS sensing and actuation (qualitative)
Given a MEMS structure, design the process flow
MEMS-CMOS Integration Sequence - Interleaved, MEMS-first, MEMS-last

Lab Questions
All processing equipments and steps used in lab to fabricate the EE143 chip
Rationale of lab procedures
Interpretation of your measured lab data