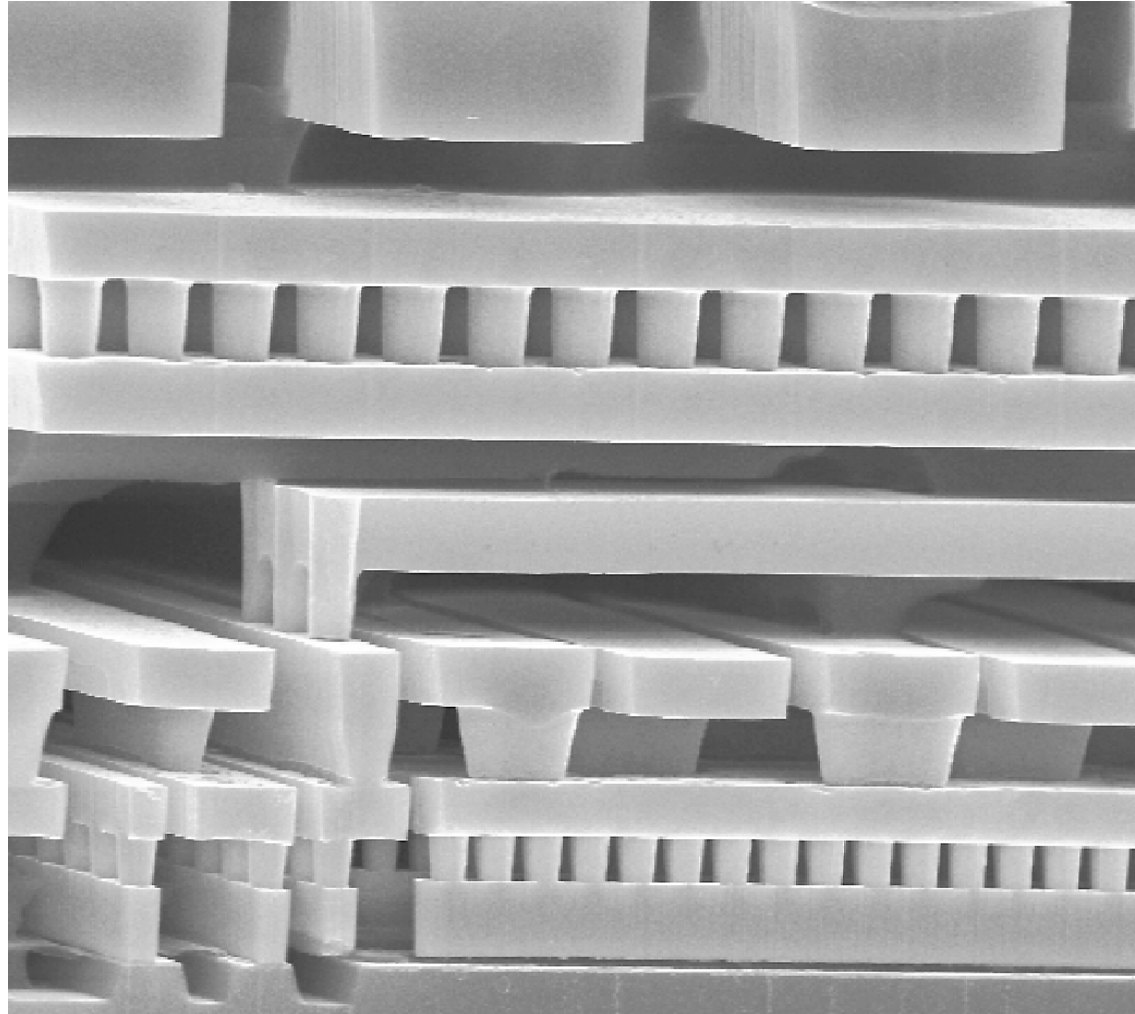


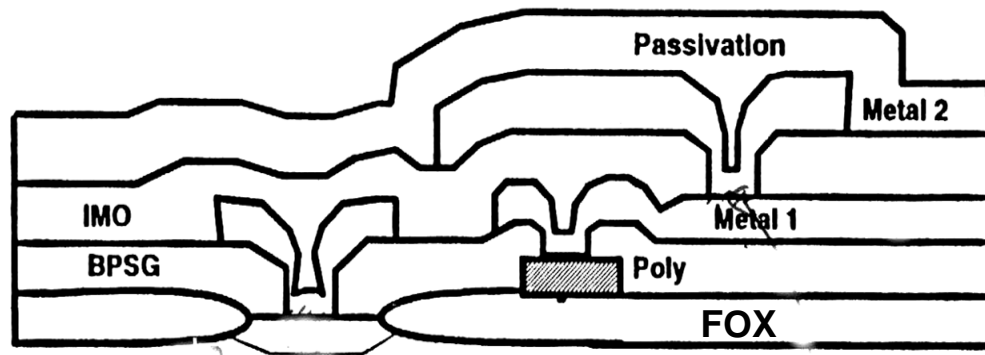
# *Section 8: Metallization*

Jaeger Chapter 7

## *Multilevel Metallization*



# *Multilevel Metallization Components*



Si substrate

- Interconnects
- Contacts - Metal to poly and doped Si
- Vias- Metal to metal contacts
- Intermetal Dielectric (Intermetal Oxide e.g. BPSG. Low-K dielectric)
- Passivation (e.g. PECVD Si Nitride)

# *Interconnect RC Time Delay*

## **Interconnect Resistance**

$$\mathbf{R_I} = R/L = \rho / (W_{Al} T_{Al})$$

## **Interconnect-Substrate Capacitance**

$$\mathbf{C_V} \equiv C/L = W_{Al} \epsilon_{ox} / T_{ox}$$

## **Interconnect-Interconnect Capacitance**

$$\mathbf{C_L} \equiv C/L = T_{Al} \epsilon_{ox} / S_{Al}$$

\* Values per unit length L

## *Interconnect Requirements*

- low ohmic resistance
  - interconnects material has low resistivity
- low contact resistance to semiconductor device
- reliable long-term operation

## *Resistivity of Metals*

TABLE 7.1 Bulk Resistivity of Metals ( $\mu\Omega\text{-cm}$ )

---

Ag: Silver	1.6
Al: Aluminum	2.65
Au: Gold	2.2
Co: Cobalt	6
Cu: Copper	1.7
Mo: Molybdenum	5
Ni: Nickel	7
Pd: Paladium	10
Pt: Platinum	10.6
Ti: Titanium	50
W: Tungsten	5

---

### Commonly Used Metals

Aluminum

Titanium

Tungsten

Copper

### Less Frequently Utilized

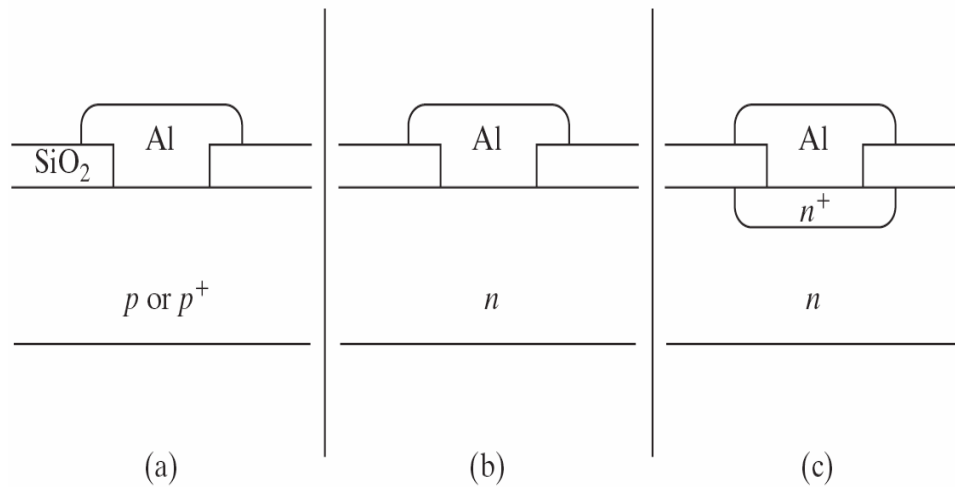
Nickel

Platinum

Paladium

Source: WebElements [<http://www.webelements.com>]

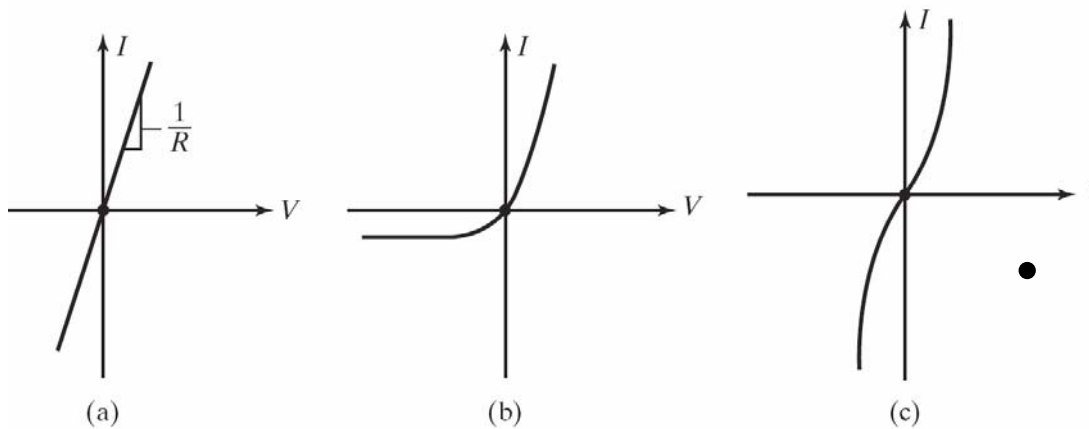
# Ohmic Contact Formation



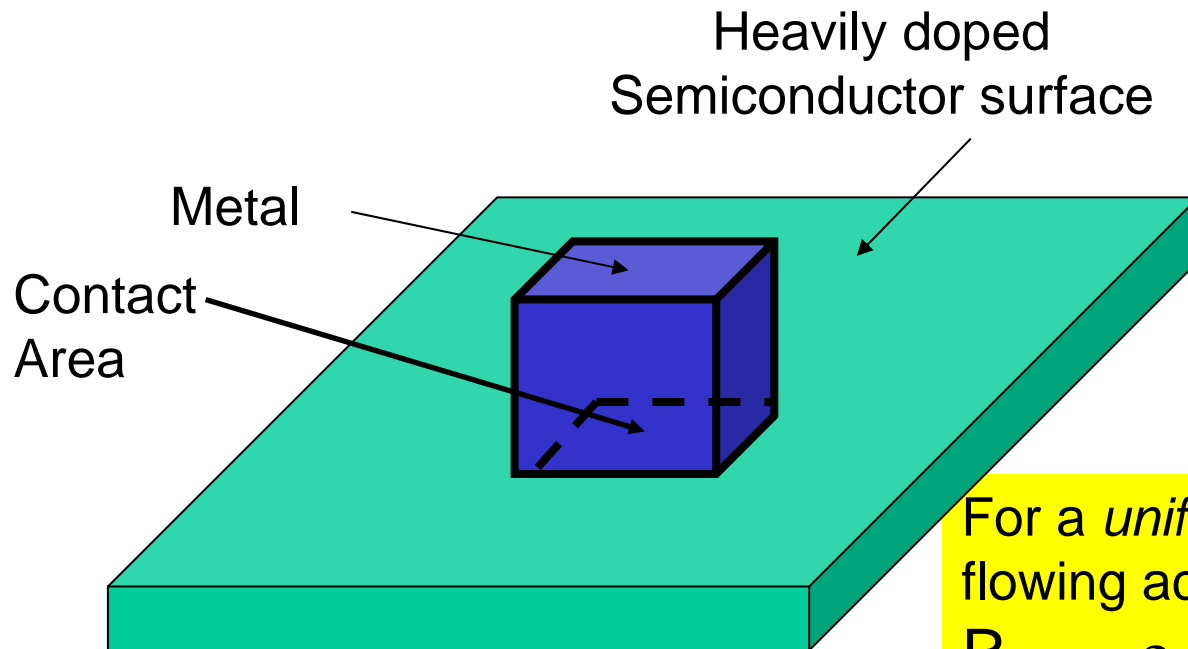
- Aluminum to p-type silicon forms an ohmic contact [Remember Al is p-type dopant]

- Aluminum to n-type silicon can form a rectifying contact (Schottky barrier diode)

- Aluminum to n<sup>+</sup> silicon yields a tunneling contact



## *Contact Resistance $R_c$*



For a *uniform* current density flowing across the contact area  
 $R_c = \rho_c / (\text{contact area})$

$\rho_c$  of Metal-Si contacts  $\sim 1\text{E-}5$  to  $1\text{E-}7 \Omega\text{-cm}^2$

$\rho_c$  of Metal-Metal contacts  $< 1\text{E-}8 \Omega\text{-cm}^2$



## *Contact Resistivity*

Specific contact resistivity  $\rho_c \equiv \left( \frac{\partial J}{\partial V} \right)^{-1}$  at  $V \sim 0$

$$\rho_c = \exp \left[ \frac{2 \sqrt{m^* \epsilon_s}}{h} \left( \frac{\phi_B}{\sqrt{N}} \right) \right]$$

$\phi_B$  is the Schottky barrier height

$N$  = surface doping concentration

$\rho_c$  = specific contact resistivity in ohm-cm<sup>2</sup>

$m$  = electron mass

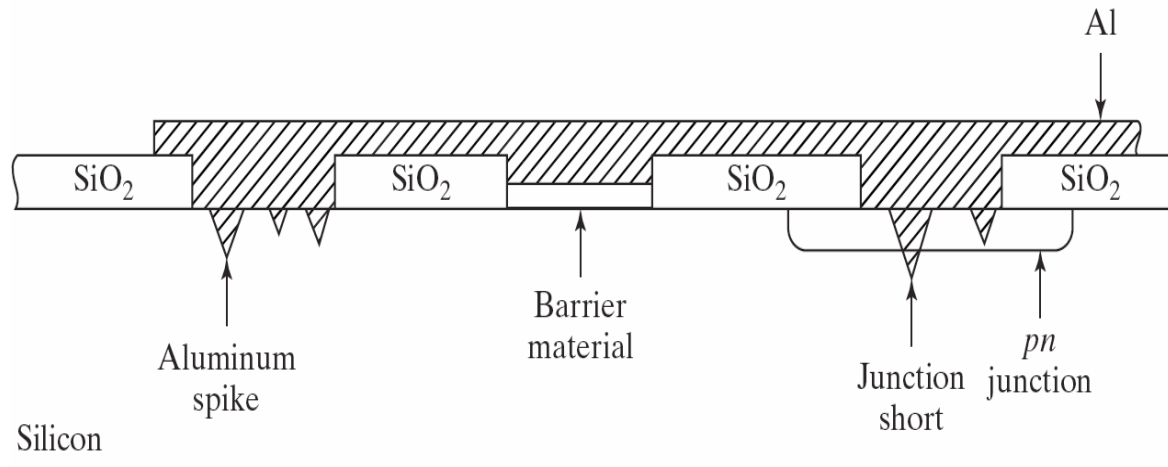
$h$  = Planck's constant

$\epsilon$  = Si dielectric constant

Approaches to lowering of contact resistance:

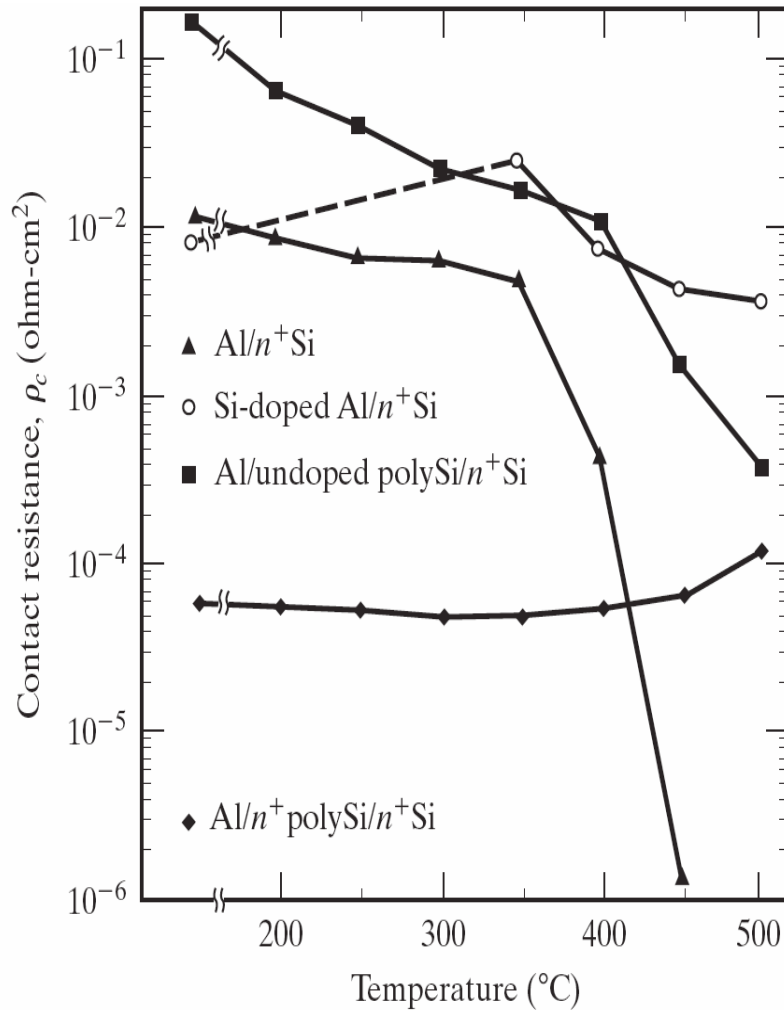
- 1) Use highly doped Si as contact semiconductor
- 2) Choose metal with lower Schottky barrier height

# *Aluminum Spiking and Junction Penetration*



- Silicon absorption into the aluminum results in aluminum spikes
- Spikes can short junctions or cause excess leakage
- Barrier metal deposited prior to metallization
- Sputter deposition of Al - 1% Si

# Alloying of Contacts



Alloy to Obtain Very Low Contact Resistivity

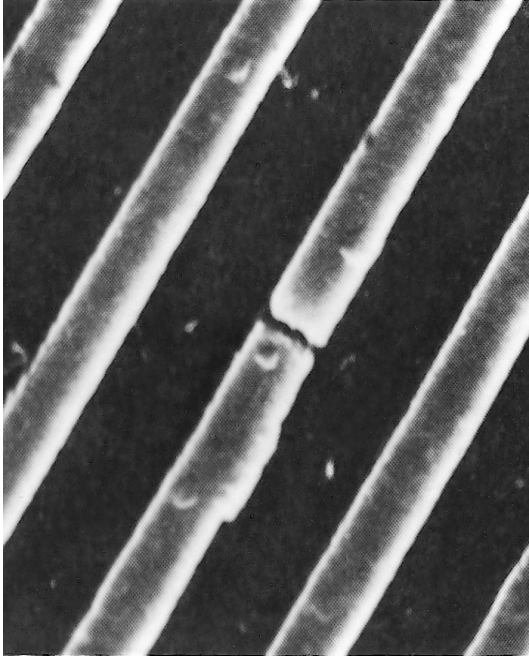
Specific Contact Resistivity

$$\rho_c = 1.2 \times 10^{-6} \Omega - cm^2$$

Contact Resistance  $R_C$

$$R_C = \frac{\rho_c}{A} \quad A = \text{contact area}$$

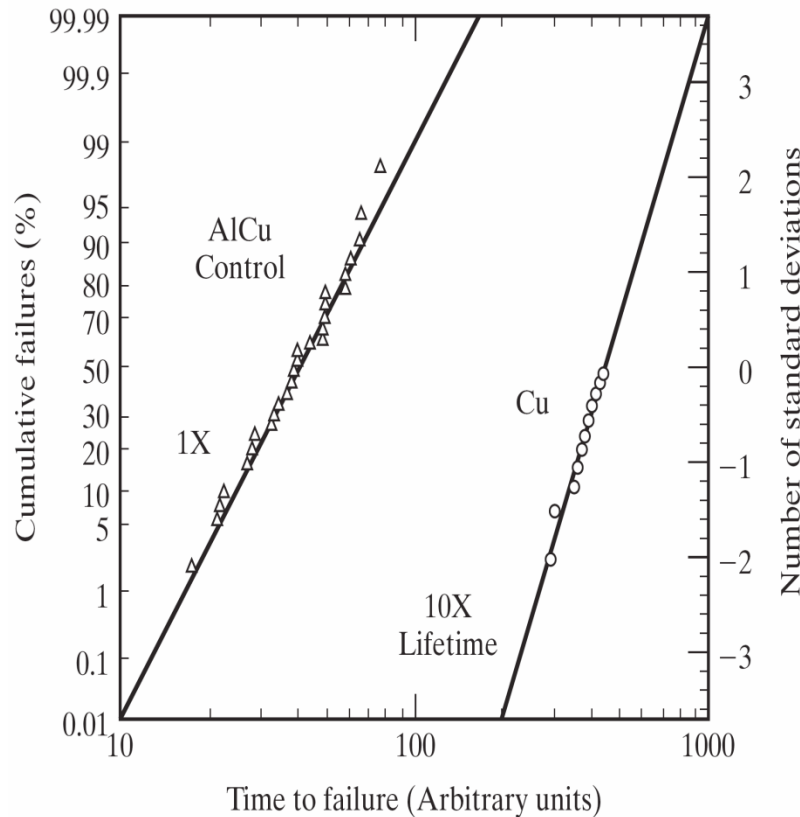
## *Electromigration*



High current density causes voids to form in interconnections

“Electron wind” causes movement of metal atoms

# Electromigration



- Copper added to aluminum to improve lifetime (Al, 4% Cu, 1% Si)

$$MTF \propto \frac{1}{J^2} \exp\left(\frac{E_A}{kT}\right)$$

$J$  = current density

$E_A$  = activation energy

MTF = mean time to failure

- Heavier metals (e. g. Cu) have lower activation energy

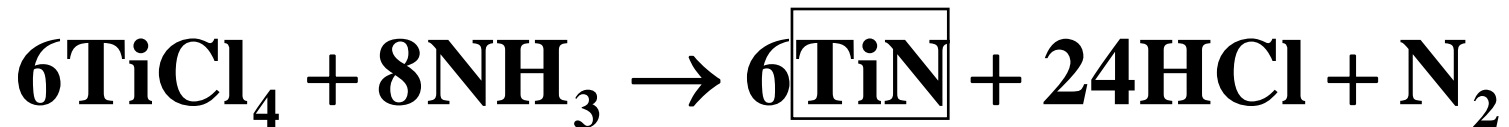
## *Metal Deposition Techniques*

- Sputtering has been the technique of choice
  - high deposition rate
  - capability to deposit complex alloy compositions
  - capability to deposit refractory metals
  - uniform deposition on large wafers
  - capability to clean contact before depositing metal
- CVD processes have recently been developed  
(*e.g.* for W, TiN, Cu)
  - better step coverage
  - selective deposition is possible
  - plasma enhanced deposition is possible for lower deposition temperature

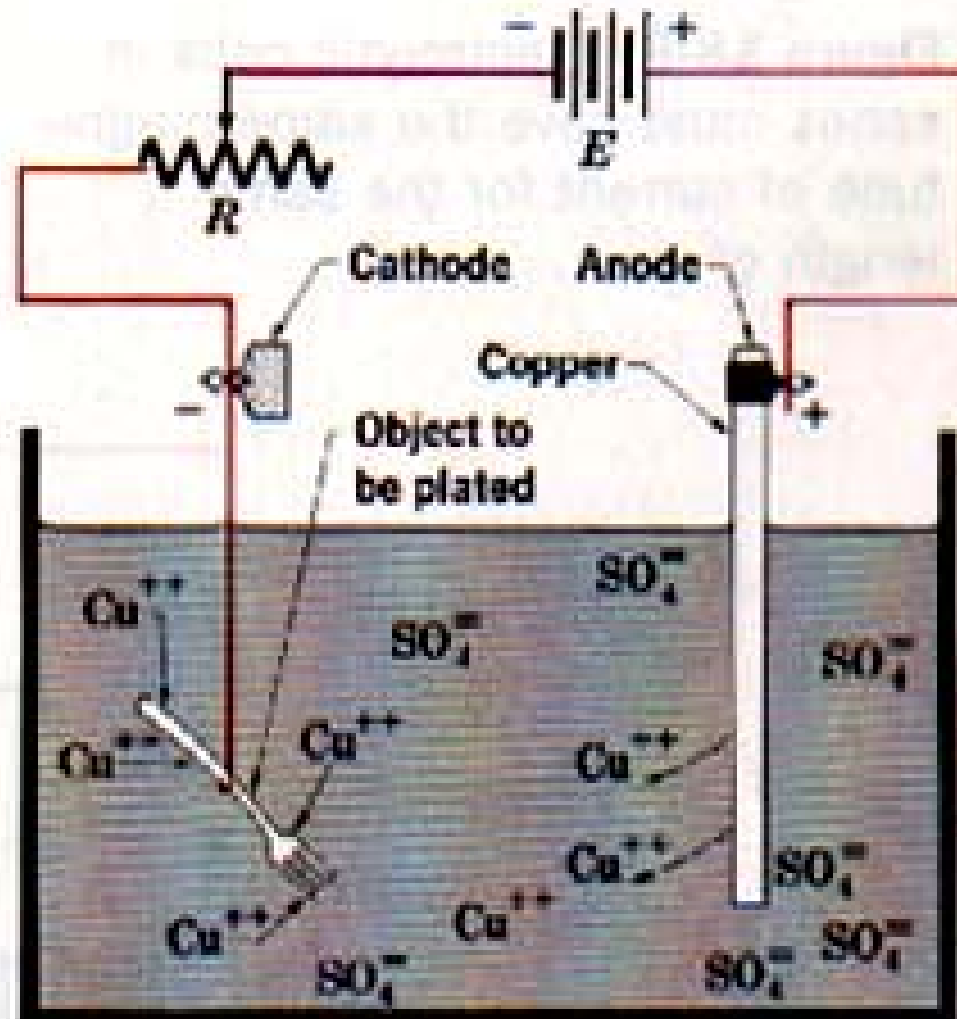
## *Metal CVD Processes*

TiN

- used as barrier-metal layer
- deposition processes:



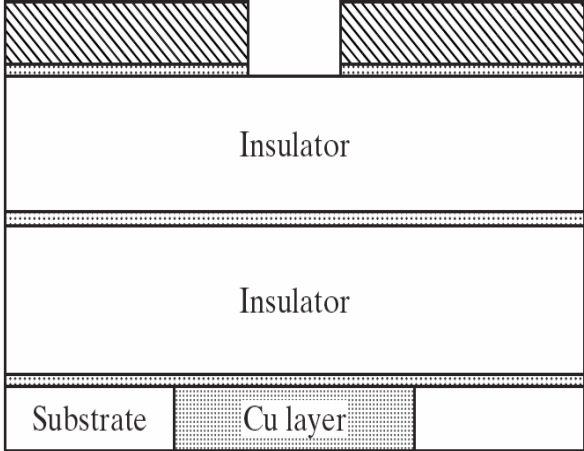
# *Electroplating*





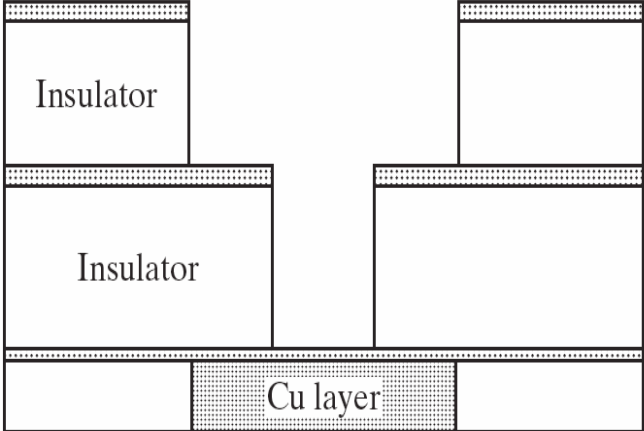
# Dual Damascene Process

Via resist



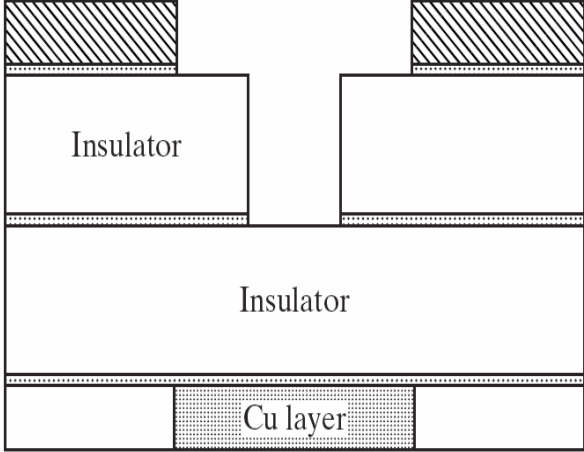
(a)

Etch stop  
( $\text{Si}_3\text{N}_4$ )



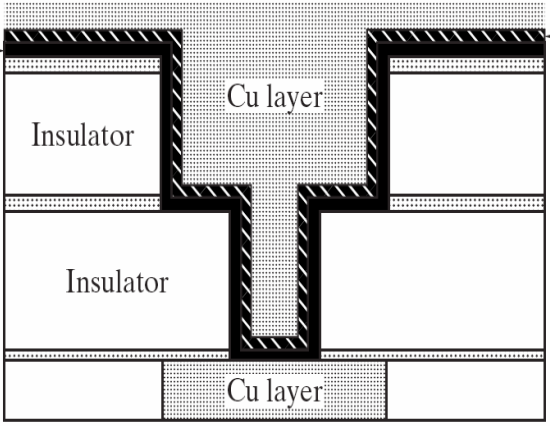
(c)

Metal resist



(b)

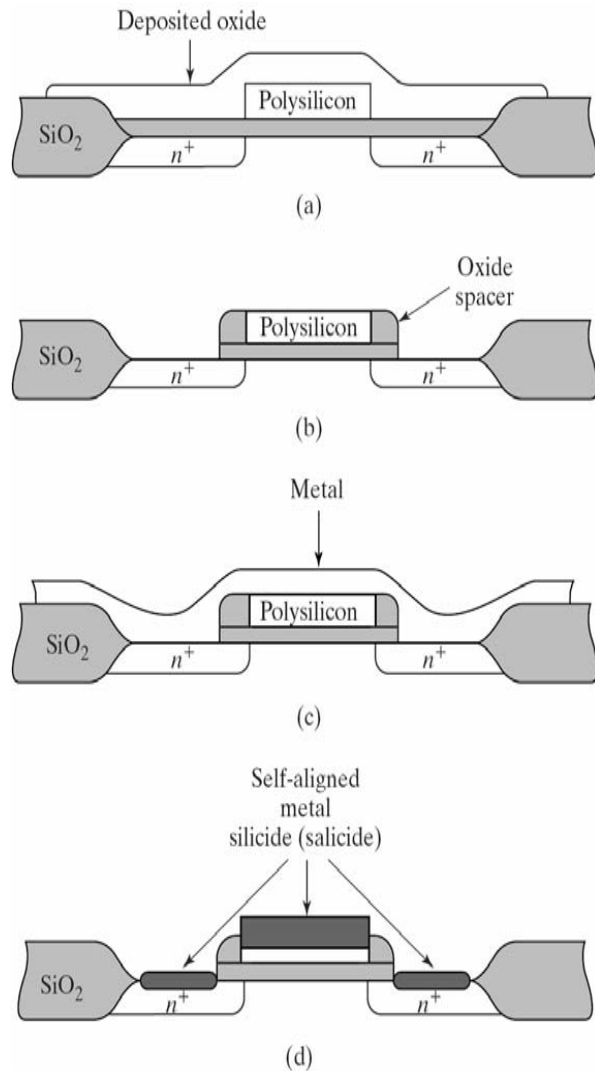
Barrier  
layer  
(TiN)



Seed  
layer

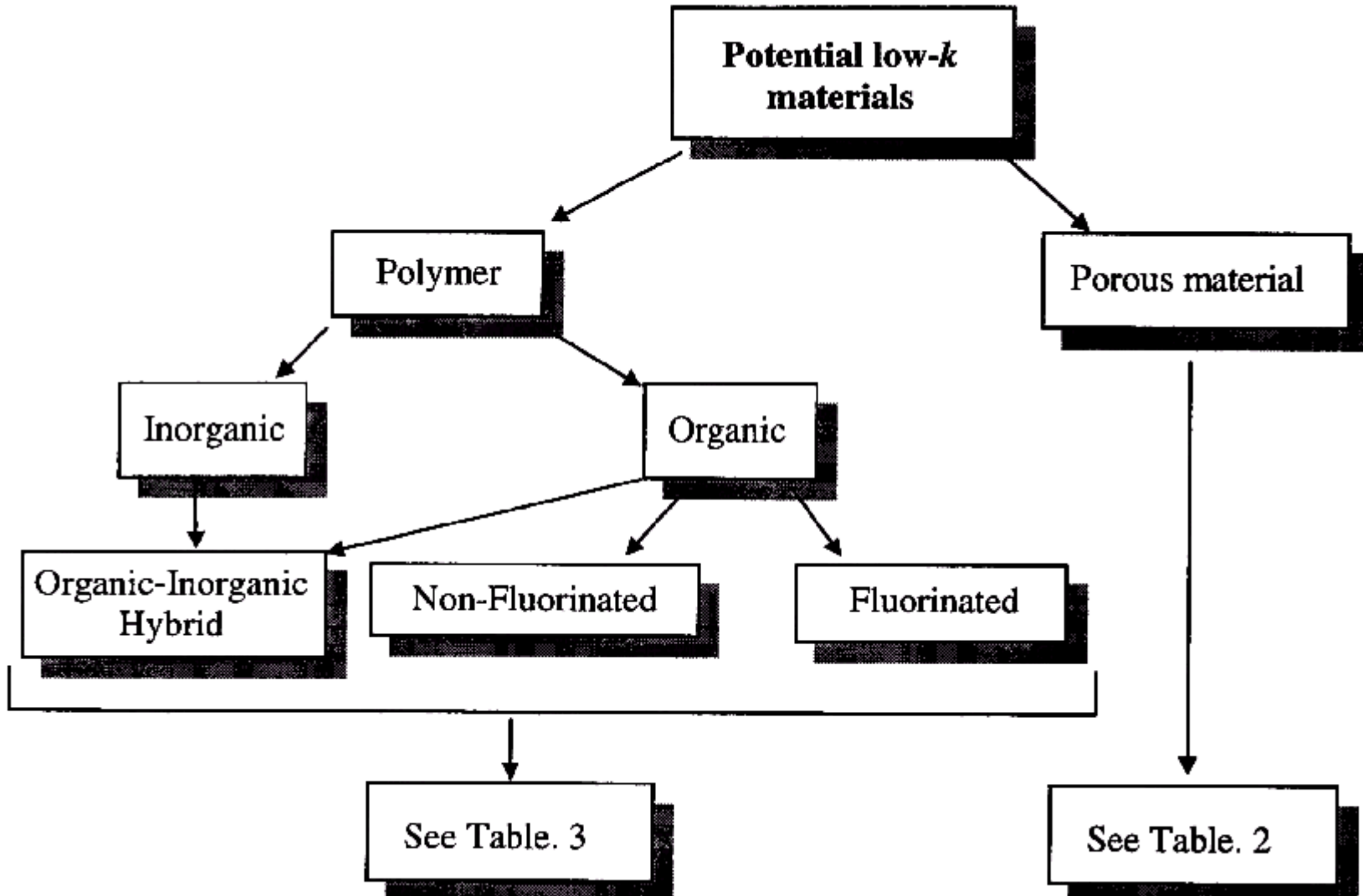
(d)

# Salicides



- Self-Aligned Silicide on silicon and polysilicon
- Often termed “Salicide”

# *Low-K Dielectrics*



## *Porous low-k dielectric examples*

<b>Materials</b>	<b>Dielectric constant</b>
TEOS* – based glass [9]	4.2
Fluorinated high-density plasma oxide (F-HDP) [10]	3.5 – 3.6
Nanoporous silica [11]	1 – 2.7
Fluorinated Amorphous carbon films [12-13]	2.3 – 2.4
Hydrophobic porous SOG (HPS) [14]	2.5
Xerogels & aerogels [4,15-17]	1.3 – 3.0
Air [9]	1.0 – 2.0