Process Integration

Self-aligned Techniques
- LOCOS- self-aligned channel stop
- Self-aligned Source/Drain
- Lightly Doped Drain (LDD)
- Self-aligned silicide (SALICIDE)
- Self-aligned oxide gap

MEMS Release Techniques
- Sacrificial Layer Removal
- Substrate Undercut

Example IC Process Flows

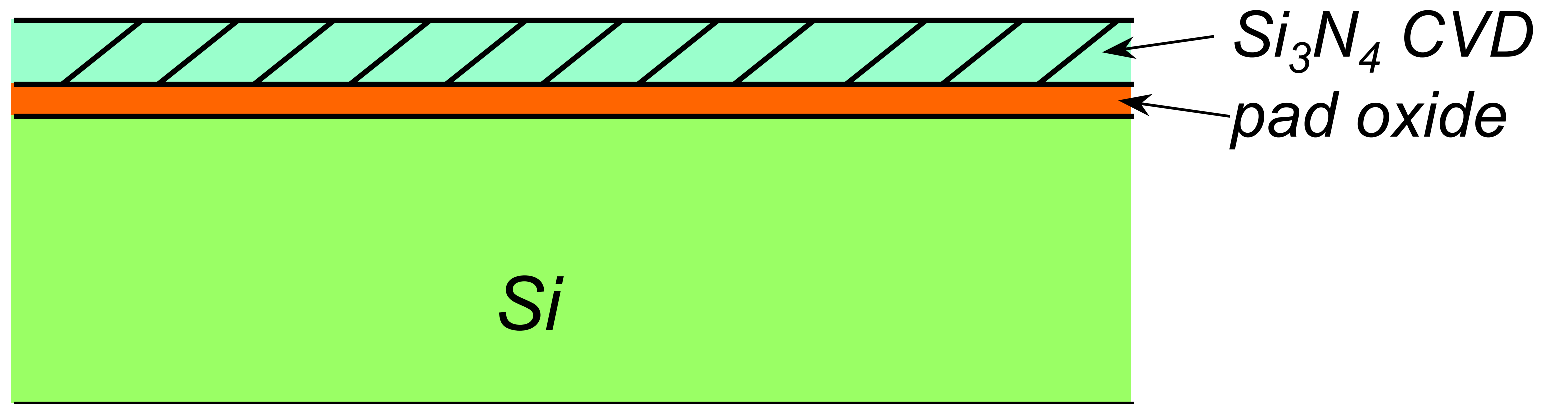
- NMOS - Generic NMOS Process Flow
- CMOS - The MOSIS Process Flow

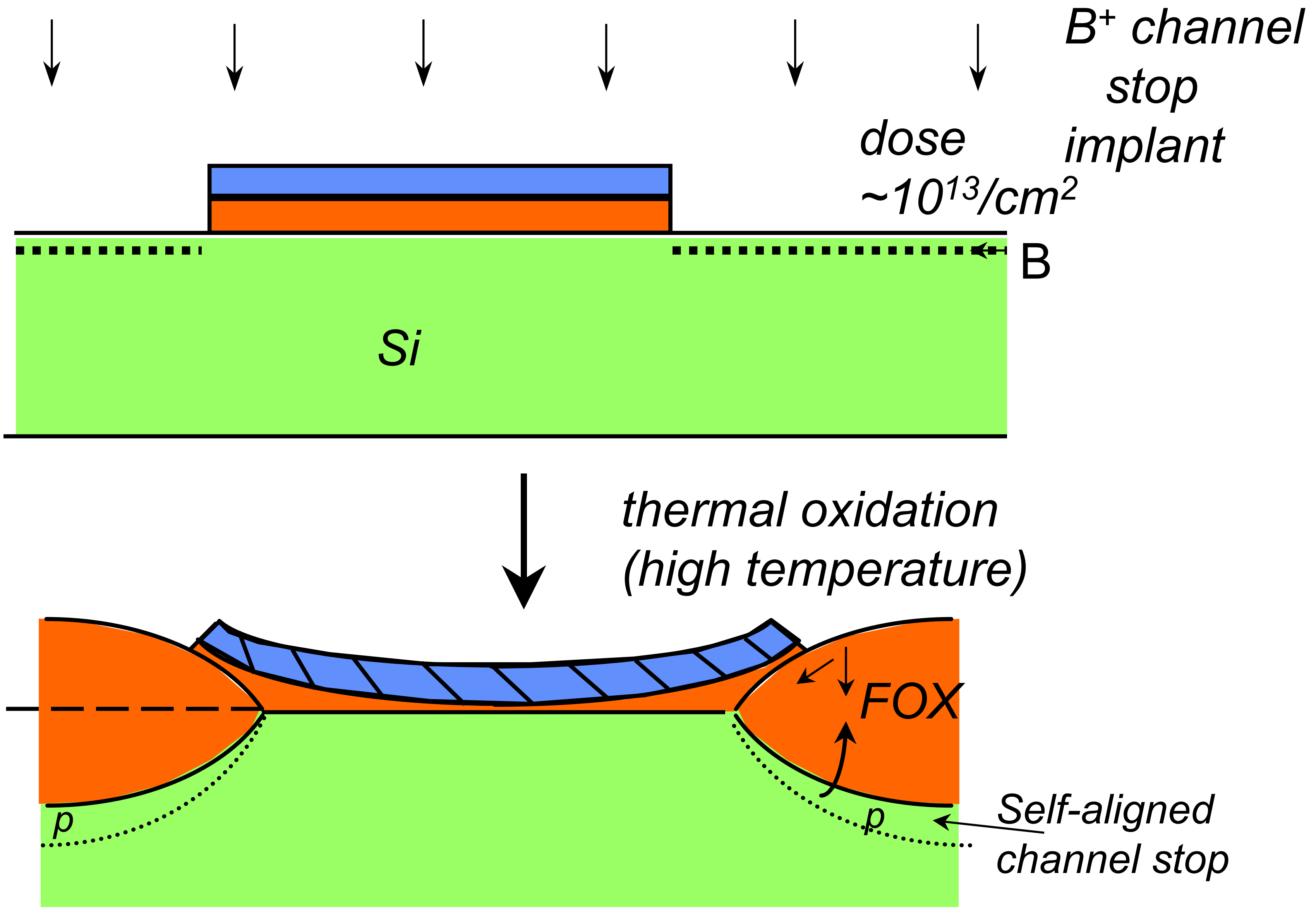
Advance MOS Techniques

- Twin Well CMOS , Retrograde Wells , SOI CMOS

Self-aligned channel stop with Local Oxidation (LOCOS)

LOCOS Process Flow

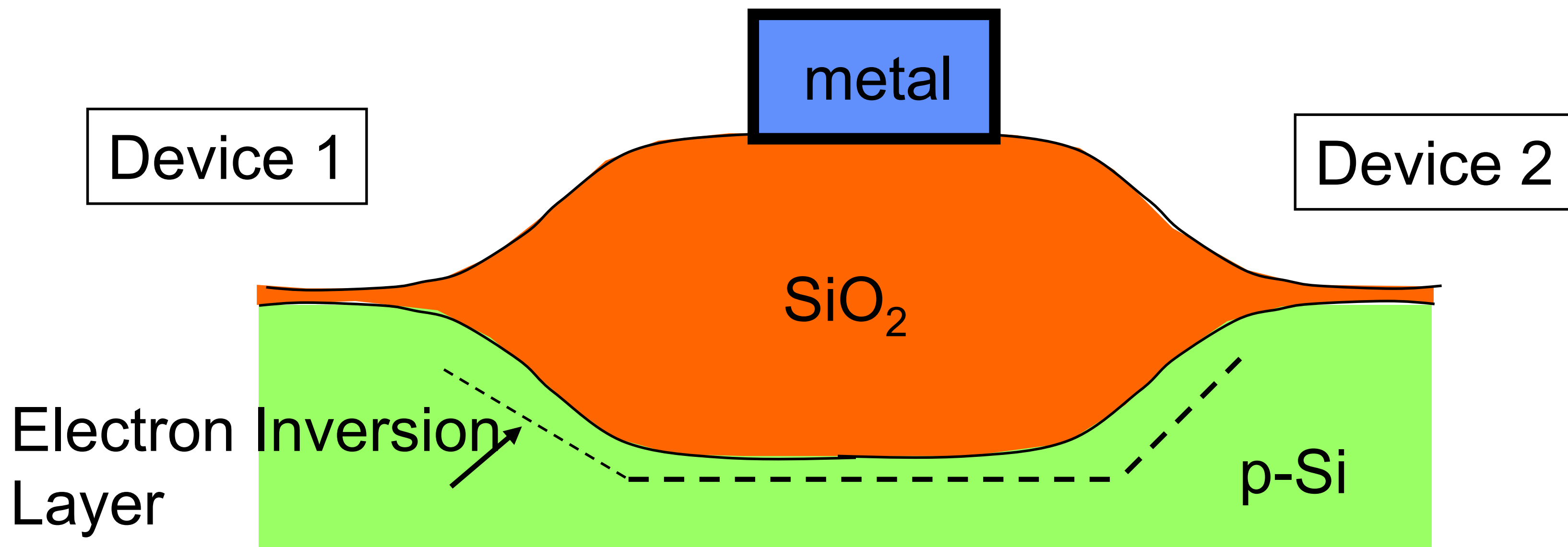




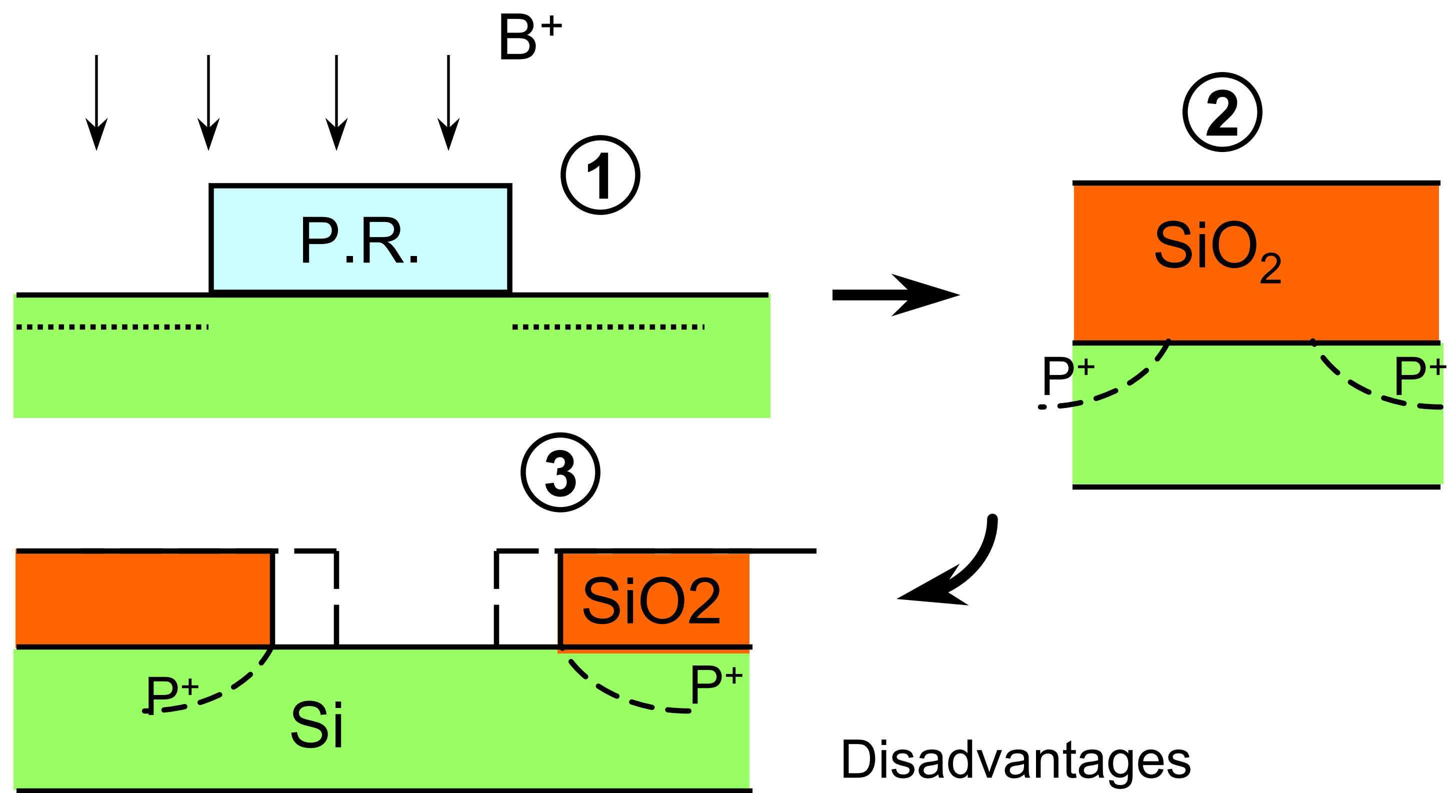
B+ channel stop implant
dose ~10^13/cm^2
B
Si
thermal oxidation (high temperature)
FOX
p
p
Self-aligned channel stop

Comment: Channel Inversion

If poly or metal lines lie on top of the FOX, they will form a parasitic MOS structure.If these lines carrying a high voltage, they may create an inversion layer of free electrons at the Si substrate and shorts out neighboring devices. **The relatively highly doped Si underneath (the “channel stop”) raises the threshold voltage needed for the inversion.**

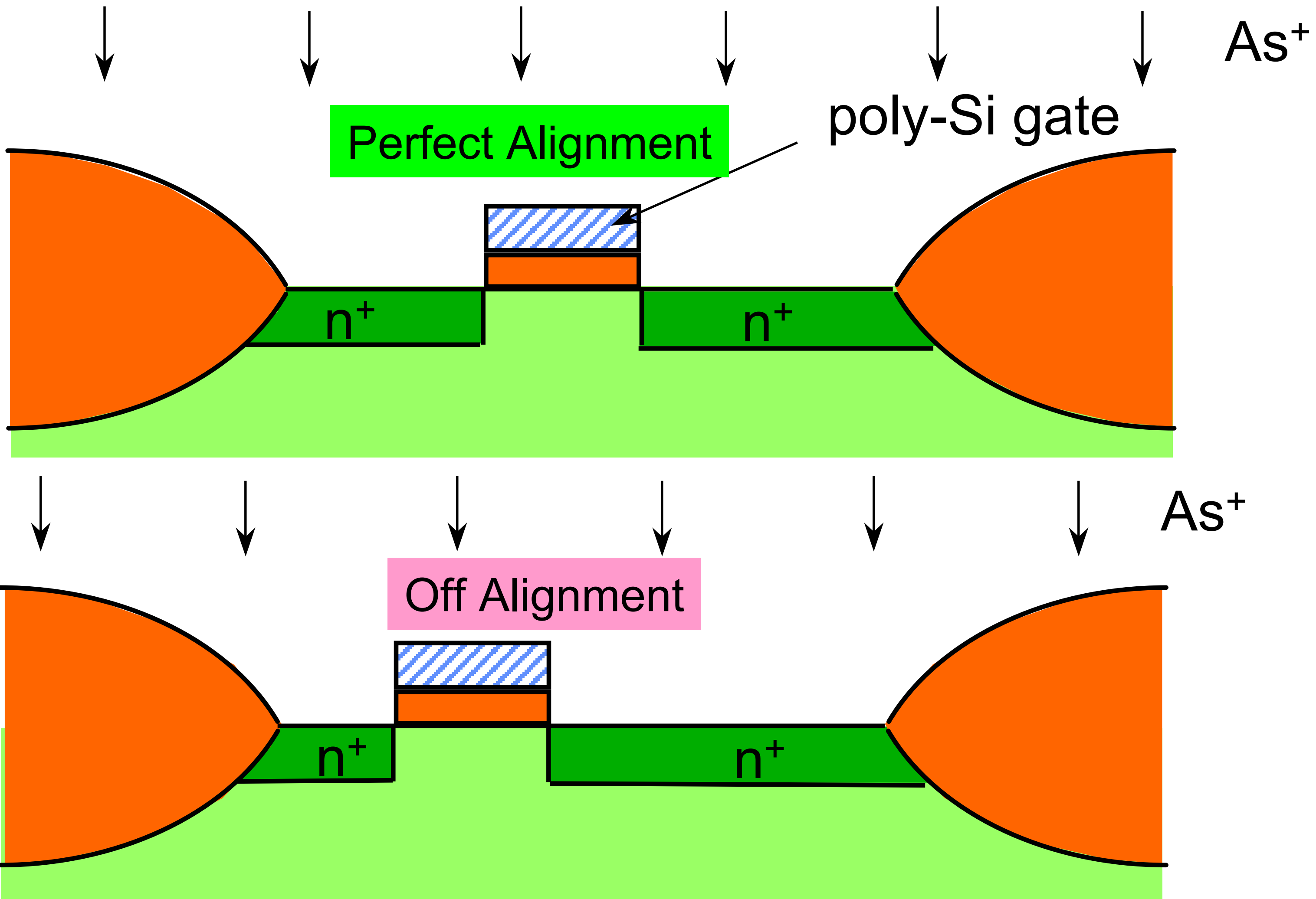


Comments : Non self-aligned alternative:



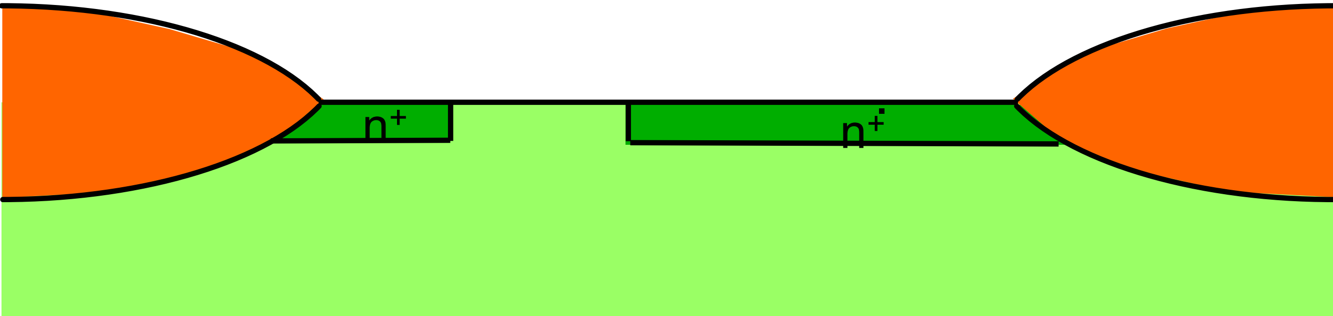
Disadvantages
1 Two lithography steps
2 Channel stop doping not FOX aligned

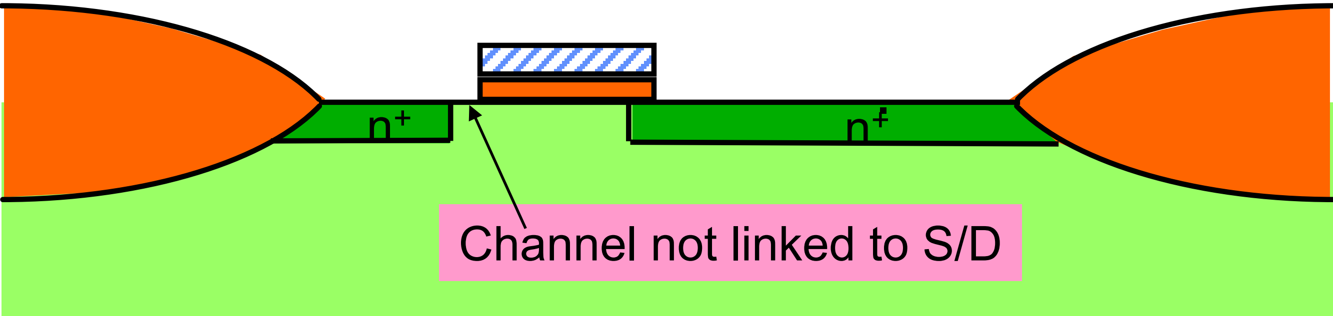
Self-aligned Source and Drain

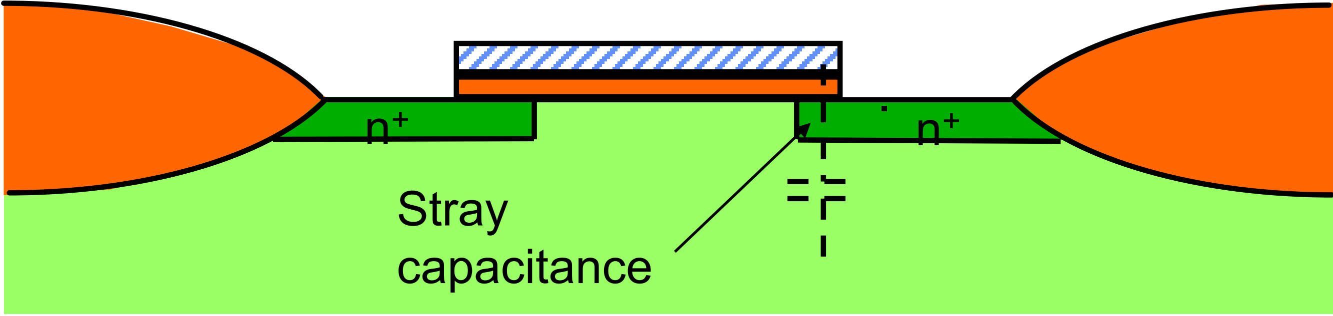


* The n+ S/D always follows gate

Comment: Non self-aligned Alternative



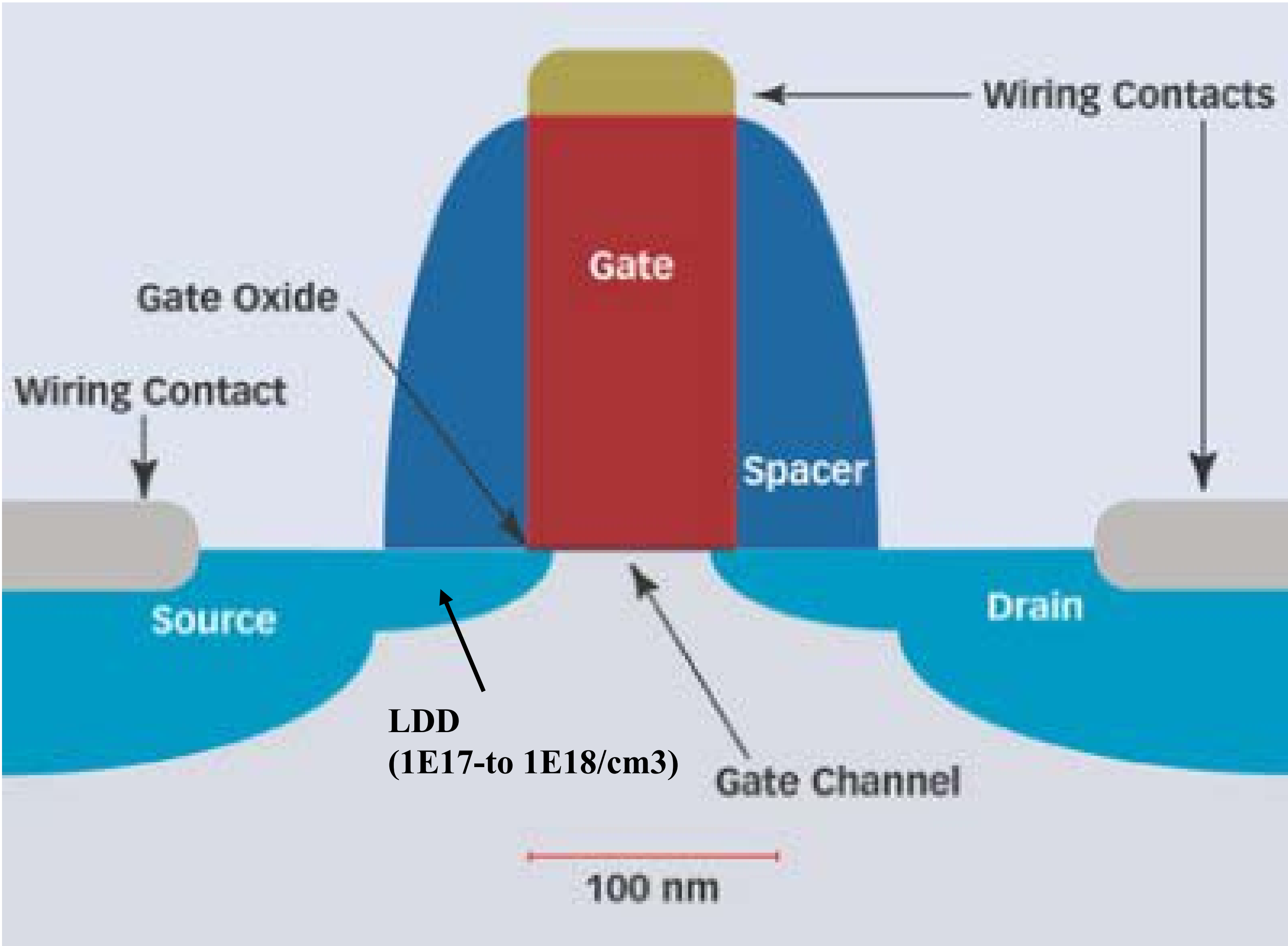




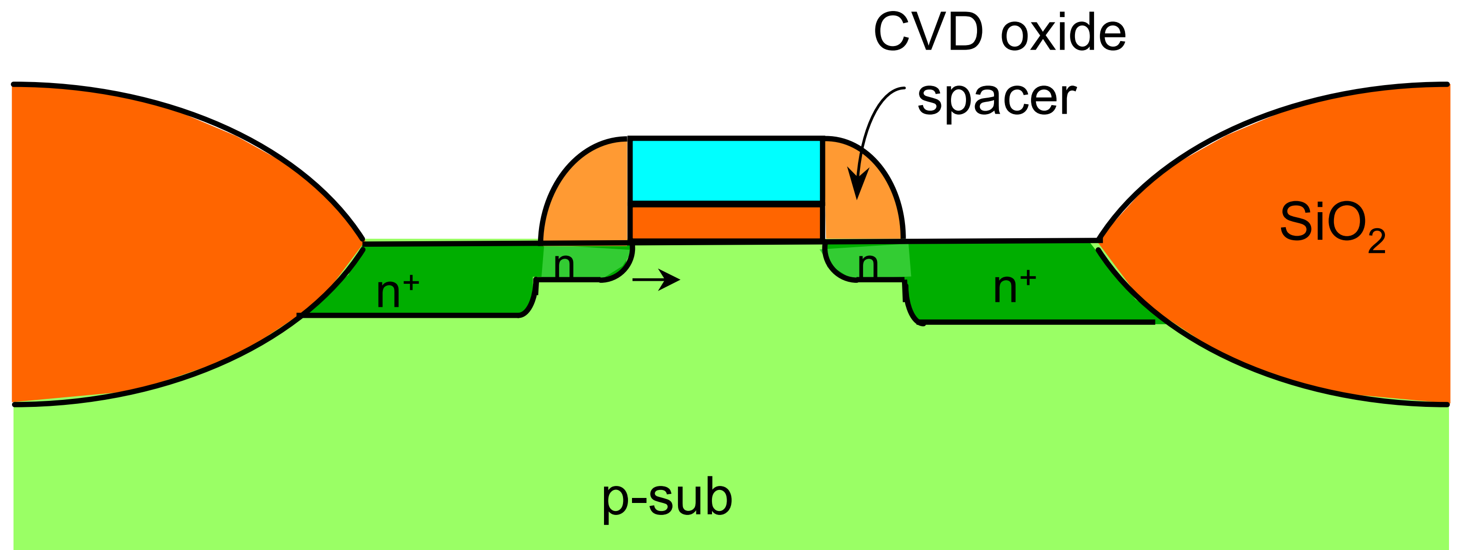
Solution: Use gate overlap to avoid offset error.

Disadvantages: Two lithography steps, excess gate overlap capacitance

Lightly Doped Drain (LDD)

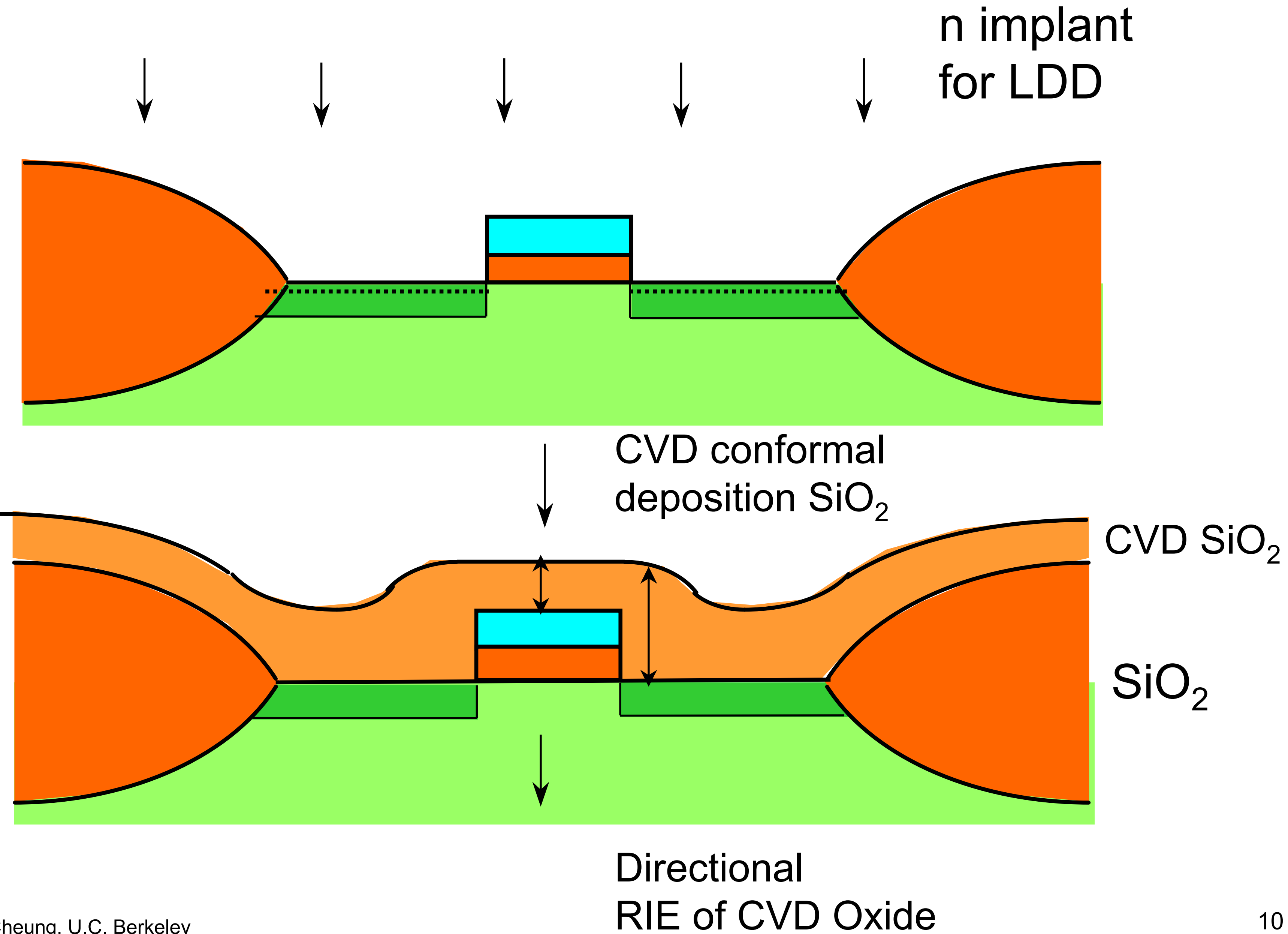


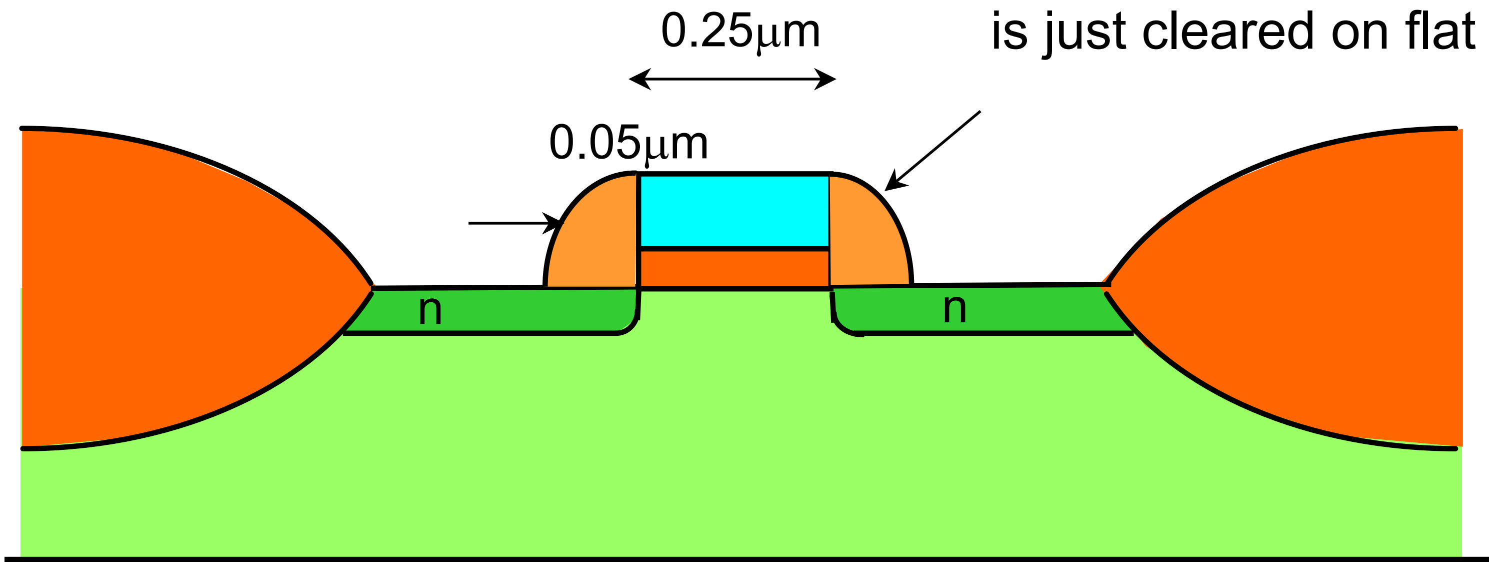
Lightly Doped Source/Drain MOSFET (LDD)



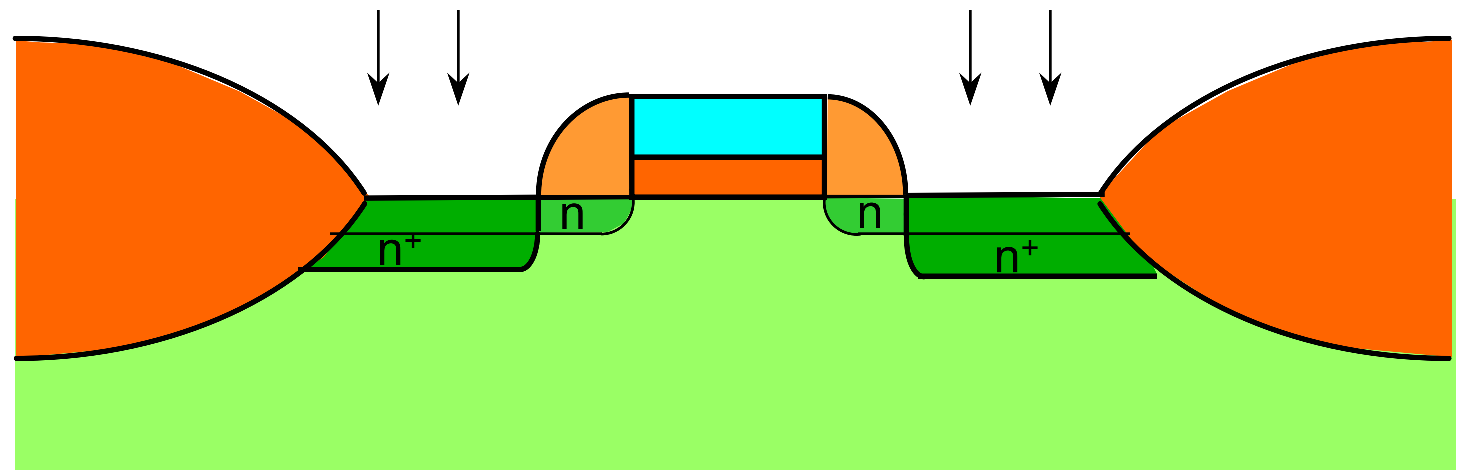
The n-pockets (LDD) doped to medium conc (~1E18) are used to smear out the strong E-field between the channel and heavily doped n+ S/D, in order to reduce hot-carrier generation.

LDD Process Flow using Ion Implantation

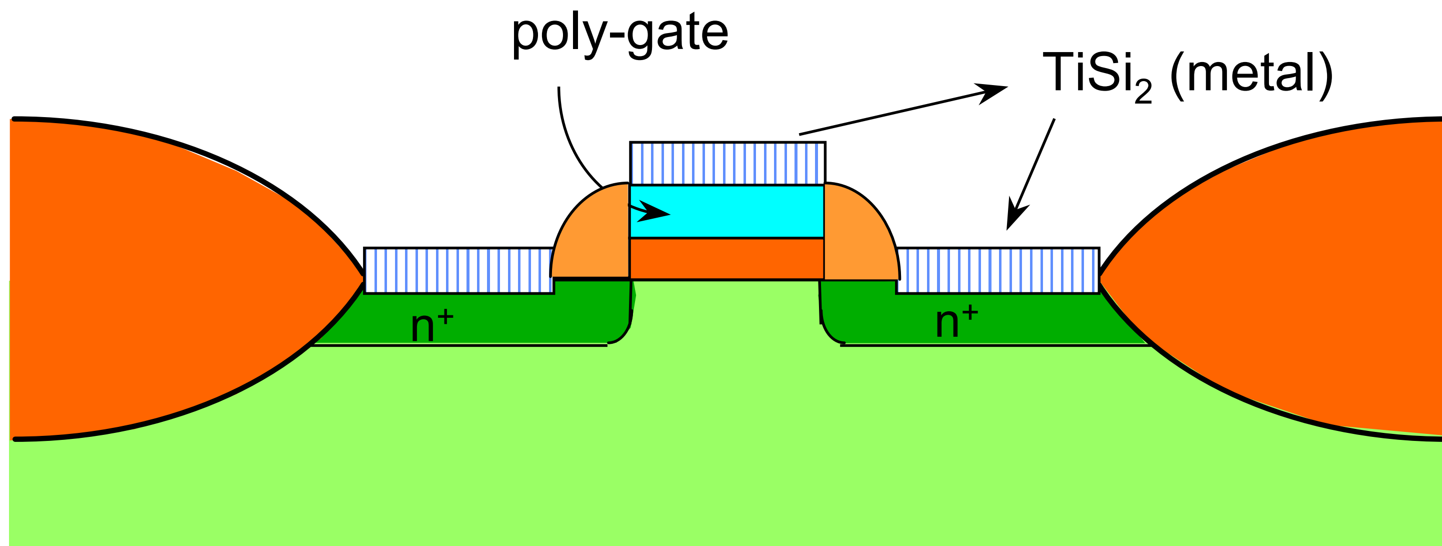




n^+ implant

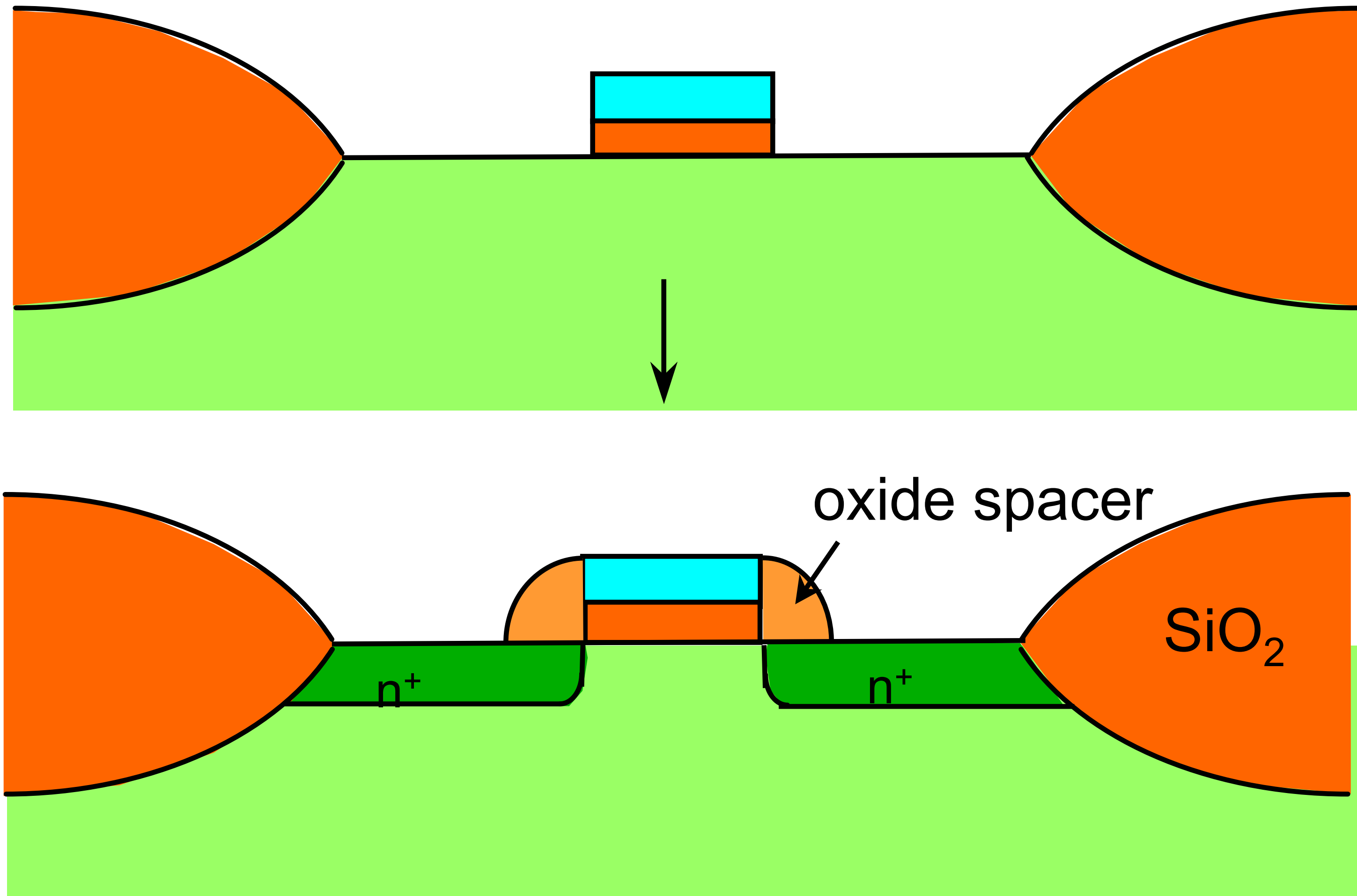


Self-Aligned Silicide Process (**SALICIDE**) using Ion Implantation and Metal-Si reaction

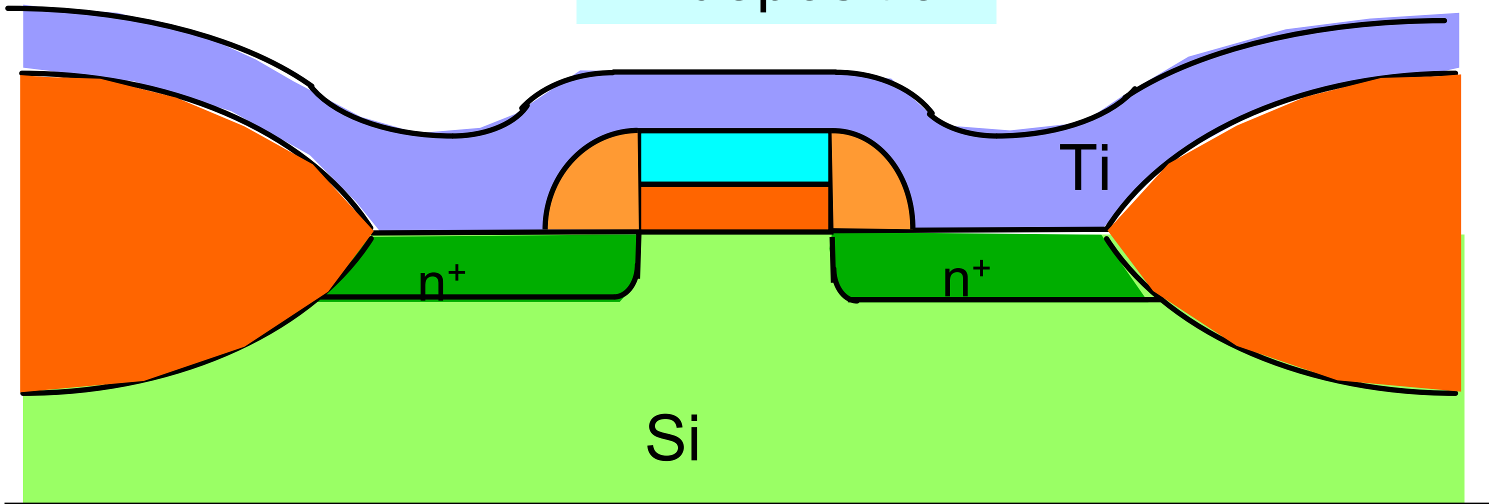


Metal silicides are metallic.
They lower the sheet resistance of S/D and the poly-gate

SALICIDE Process Flow

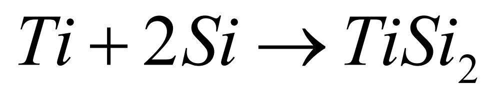


Ti deposition

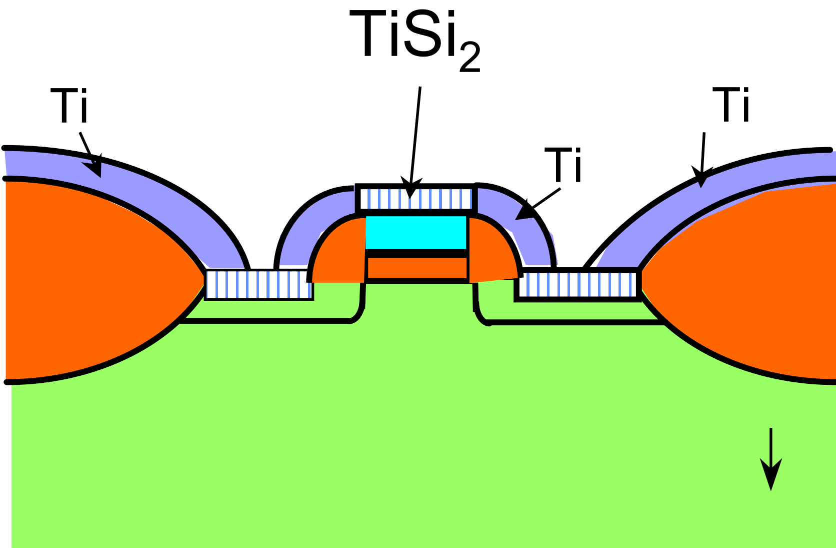


heat treatment $(> 700^{o} C)$

$$Ti + 2Si \rightarrow TiSi_2$$



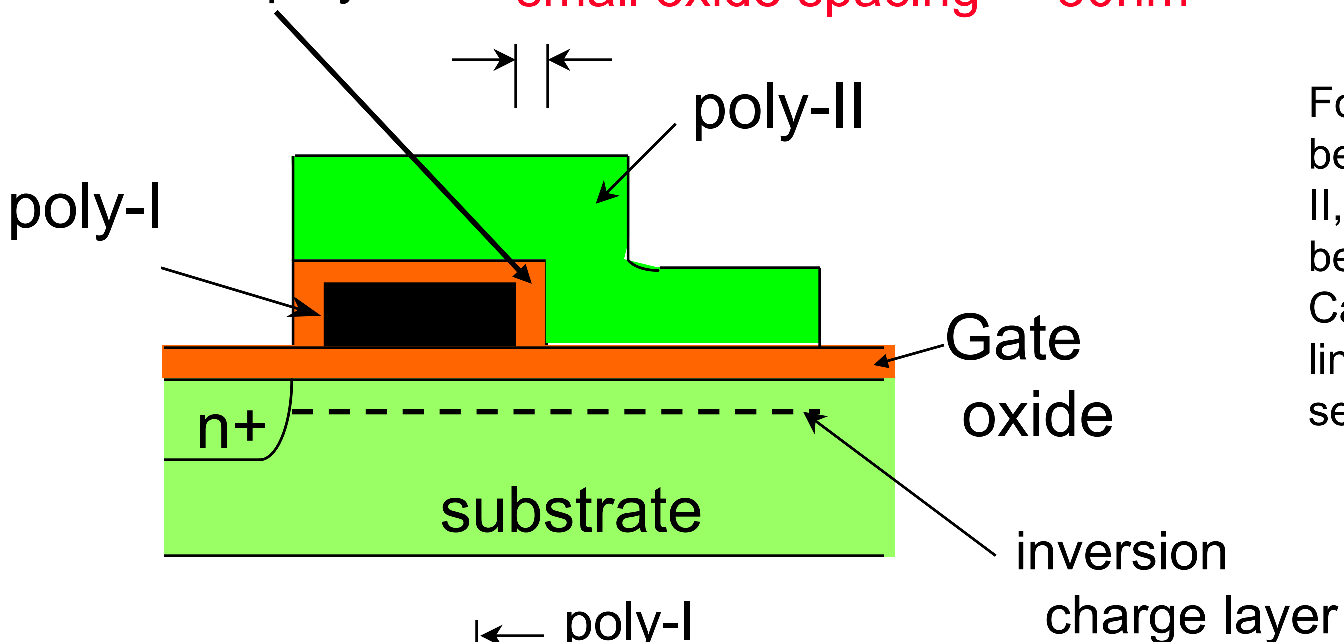
Ti will not react with SiO_2.

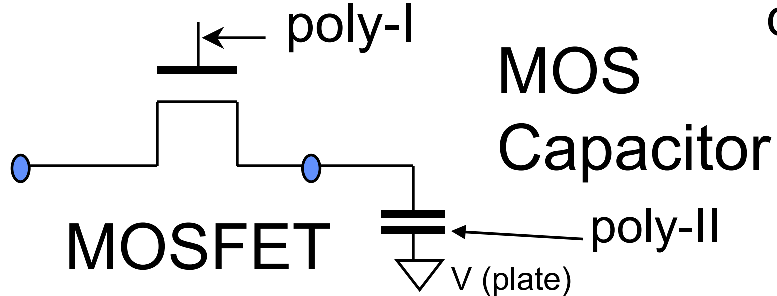


Selective etch to remove unreacted Ti only

Self-aligned Oxide Gap

DRAM structure (MOSFET with a capacitor)



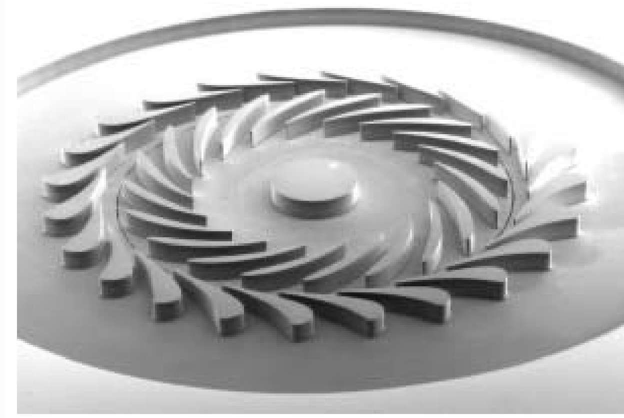


For a small spacing between poly-I and poly-II, inversion charges between MOSFET and Capacitor are electrically linked. No need for a separate n+ island.

Process Flow of MEMS Rotating Mechanisms

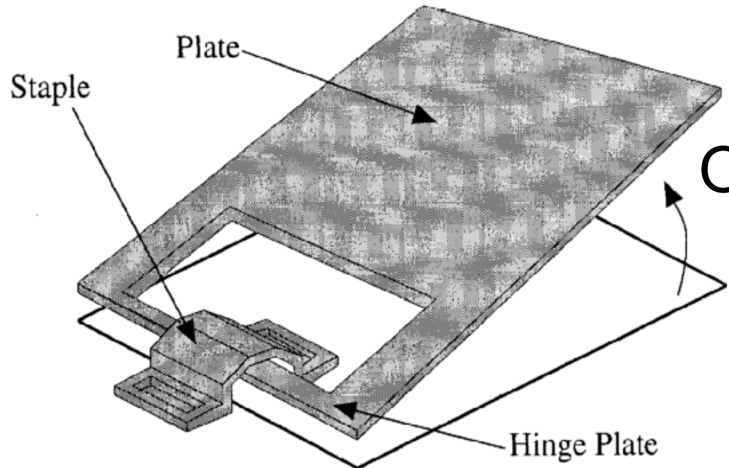
Thermal Oxide
Silicon Substrate
CVD Oxide
Polysilicon
CVD Oxide
Rotor
Shaft and Cap
Flow Channel Walls

In-Plane Movement

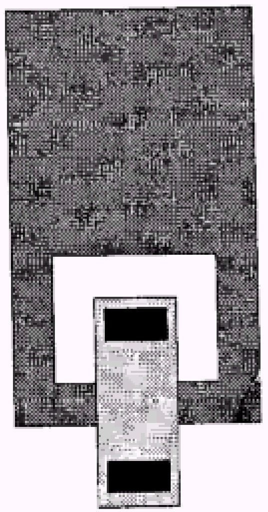


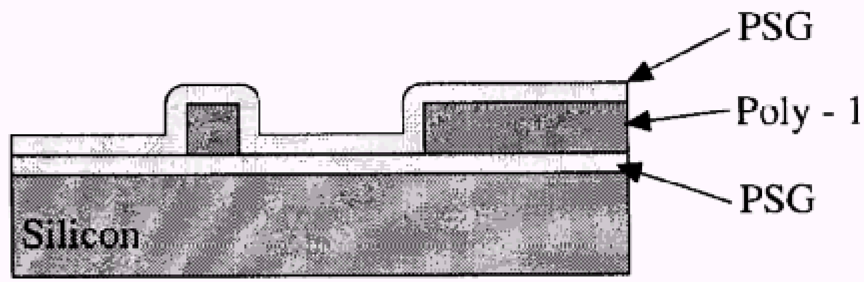
Micro-turbine Engine

Process Flow for a Hinge Structure

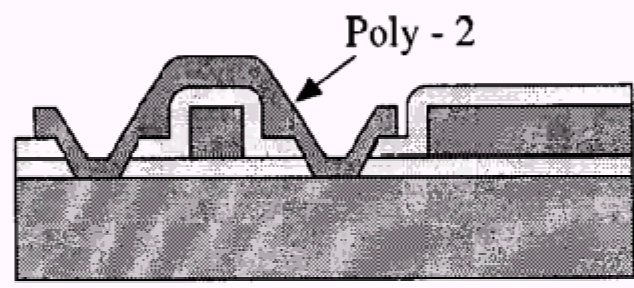


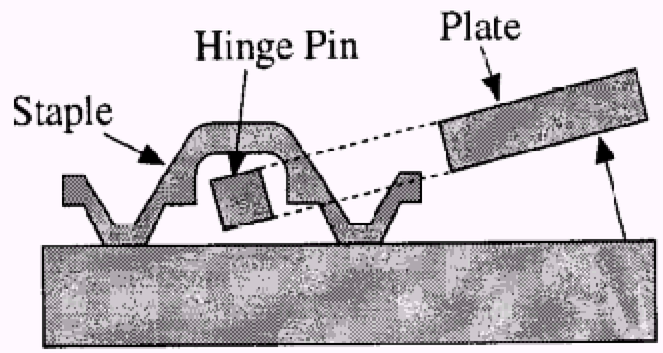
Out-of-plane Movement



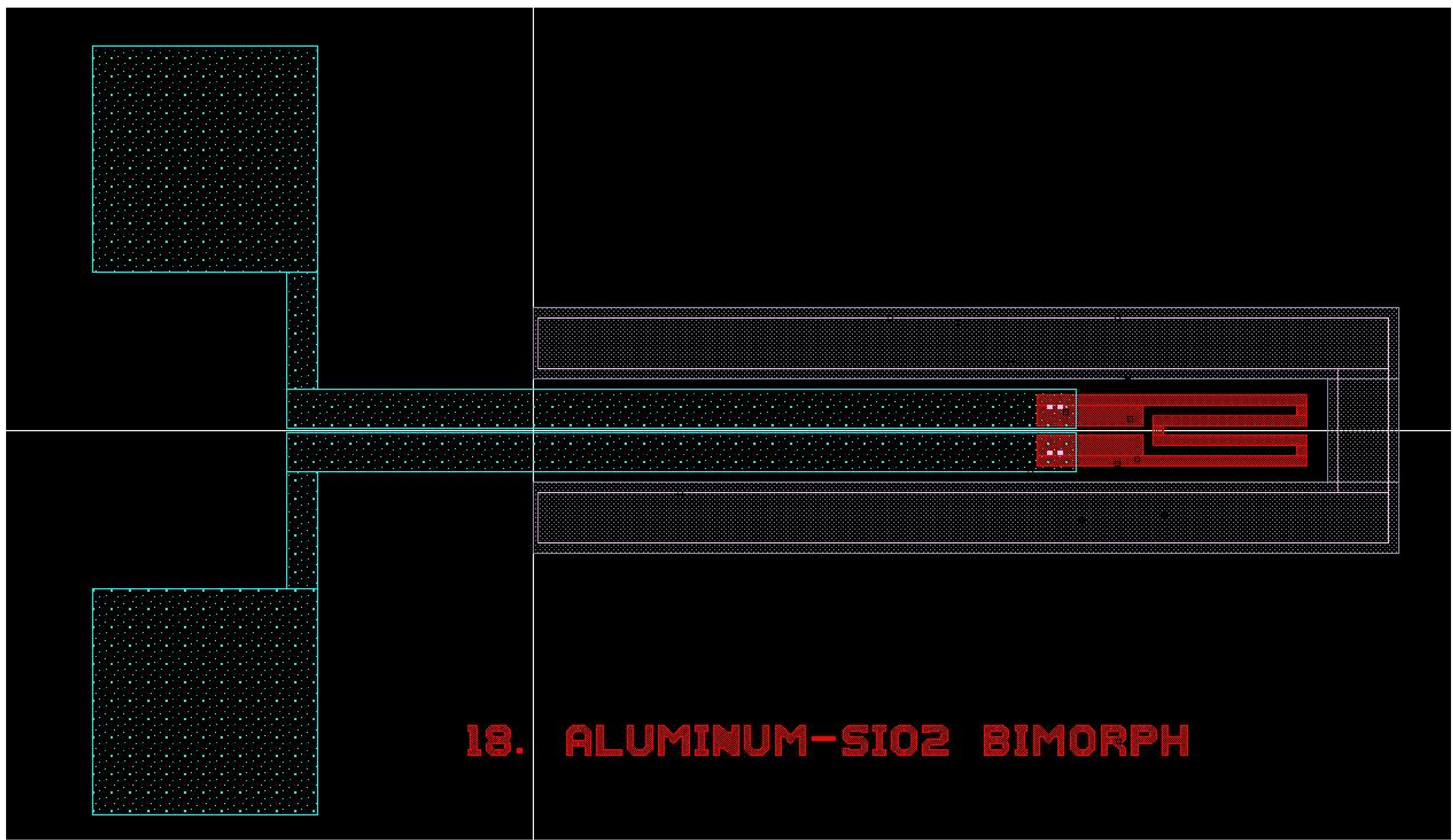


Poly - 1
Poly - 2
Contact





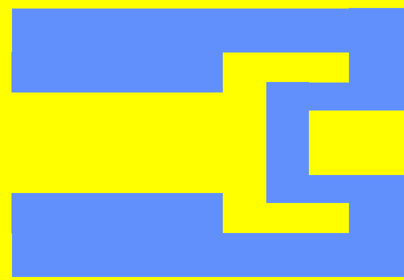
Layout of Thermal Bimorph Actuator



(See 143 Lab Manual for details)

After Patterning Poly-Si (Mask #2)

Top View



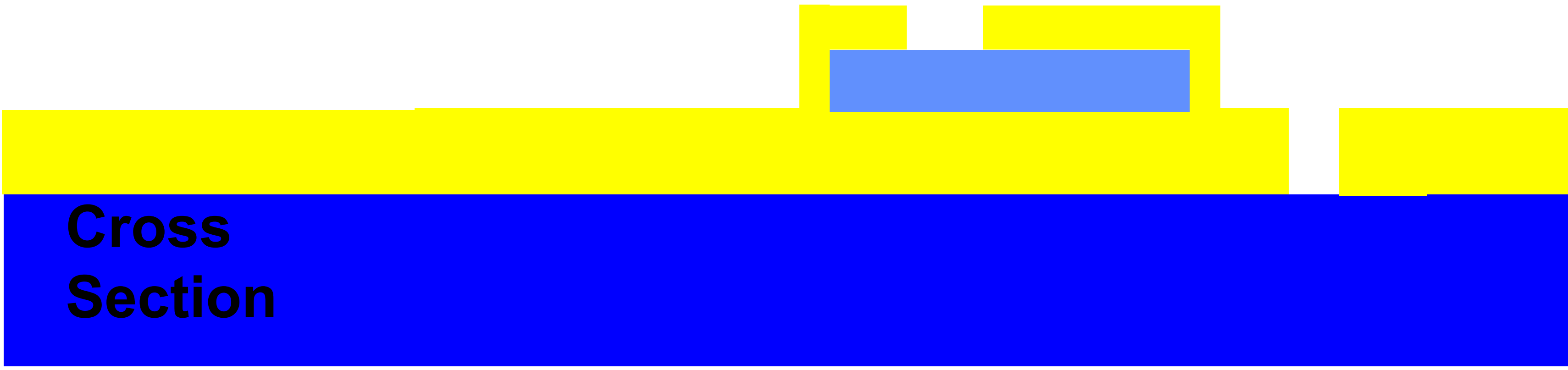
■ Aluminum ■ Poly Si ■ Oxide ■ Si substrate ☒ Al-Poly contact

Cross Section

After Patterning Intermediate Oxide (Mask #3, Contact-Hole Cut)

Top View

Aluminum Poly Si Oxide Si substrate ☒ Al-Poly contact

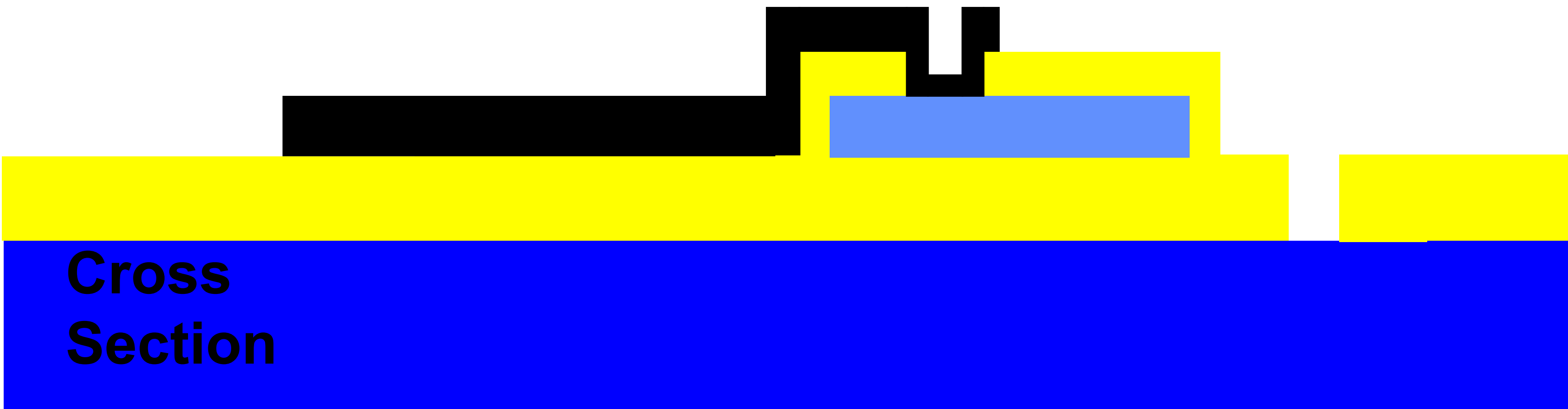


After Aluminum patterning (Mask #4)

To contact pad

Top View

■ Aluminum ■ Poly Si ■ Oxide ■ Si substrate ☒ Al-Poly contact

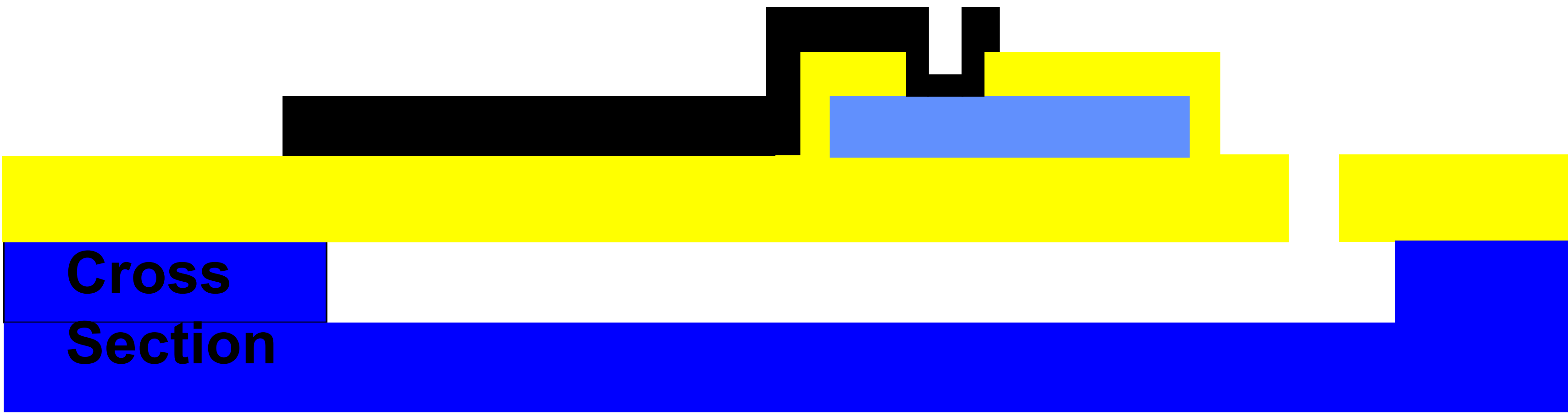


After XeF2 selective etching of Si Substrate (Final Structure)

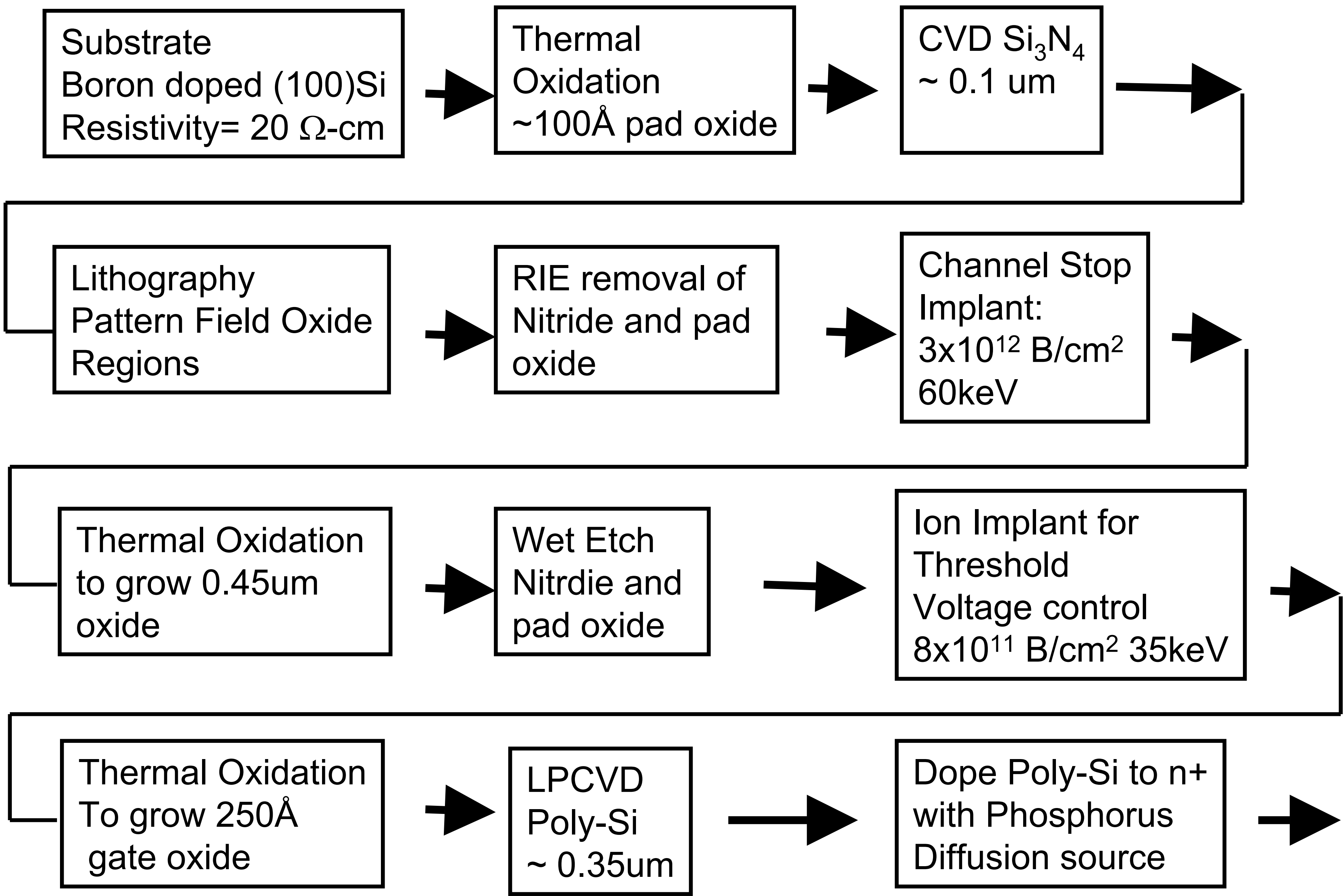
To contact pad

Top View

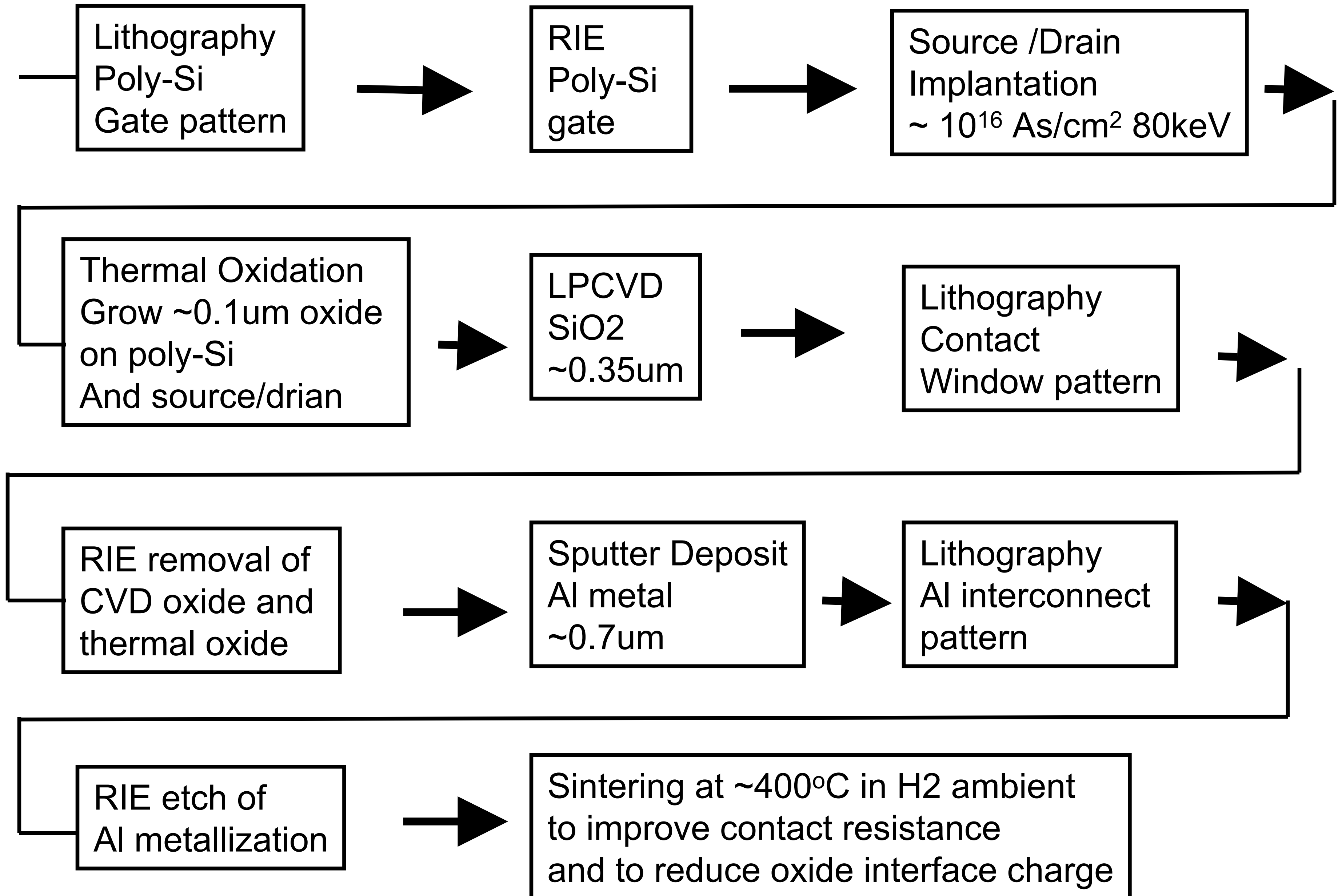
Aluminum | Poly Si | Oxide | Si substrate | ⊠ Al-Poly contact



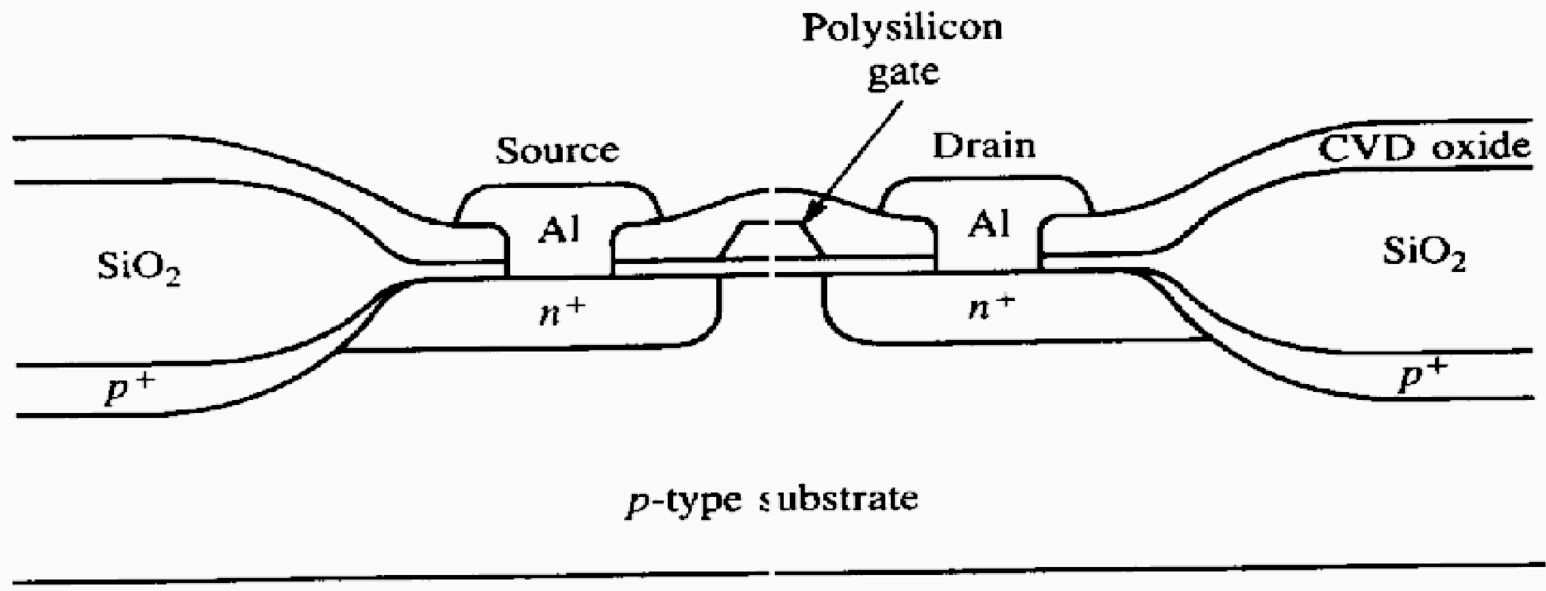
A Generic NMOS Process Flow



A Generic NMOS Process Flow (cont.)

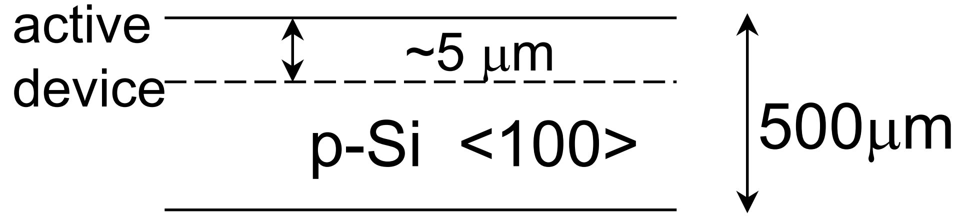


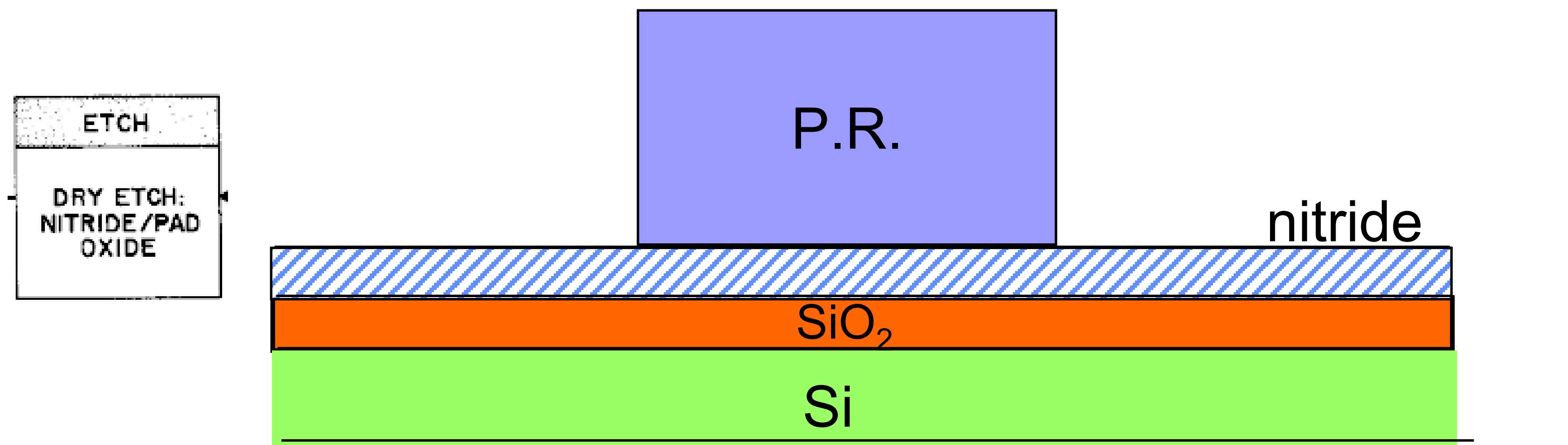
NMOS Structure

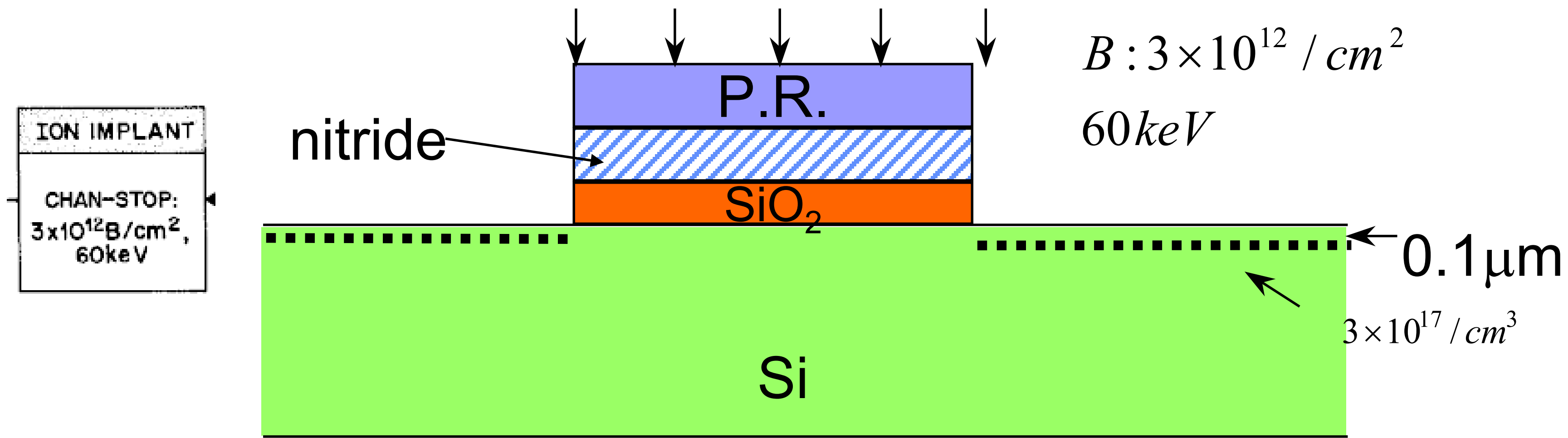


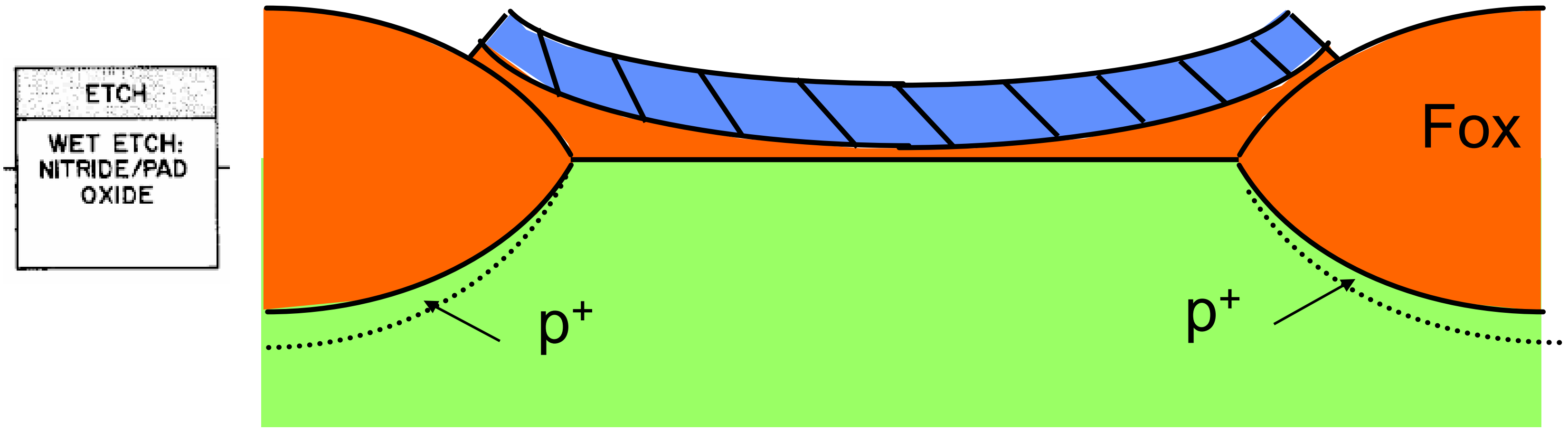
Generic NMOS Process Flow

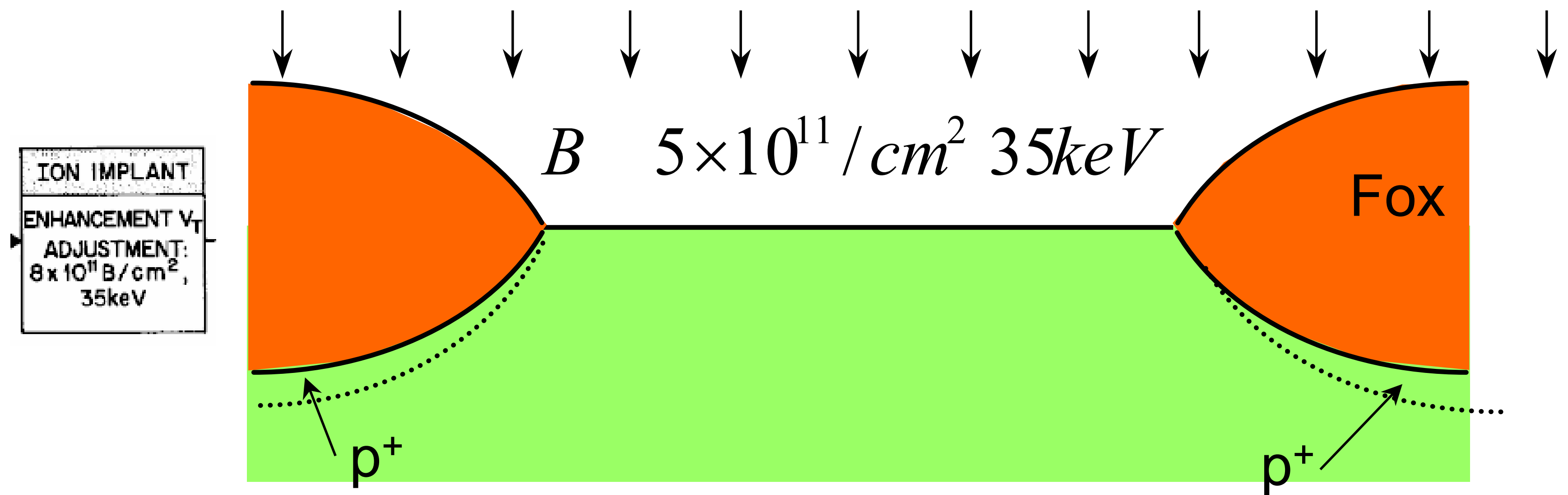
Boron-doped Si
20 Ω-cm
<100>




ETCH
DRY ETCH: NITRIDE/PAD OXIDE
P.R.
nitride
SiO2
Si


ION IMPLANT
CHAN-STOP: 3x10^12 B/cm^2, 60keV
P.R.
nitride
SiO2
Si
B : 3×10^12 / cm^2
60keV
0.1μm
3×10^17 / cm^3


ETCH
WET ETCH: NITRIDE/PAD OXIDE
Fox
p+
p+


ION IMPLANT
ENHANCEMENT V_T ADJUSTMENT: 8×10^{11} B/cm^2, 35keV
$B \quad 5\times10^{11}/cm^2 \ 35keV$
Fox
p+
p+

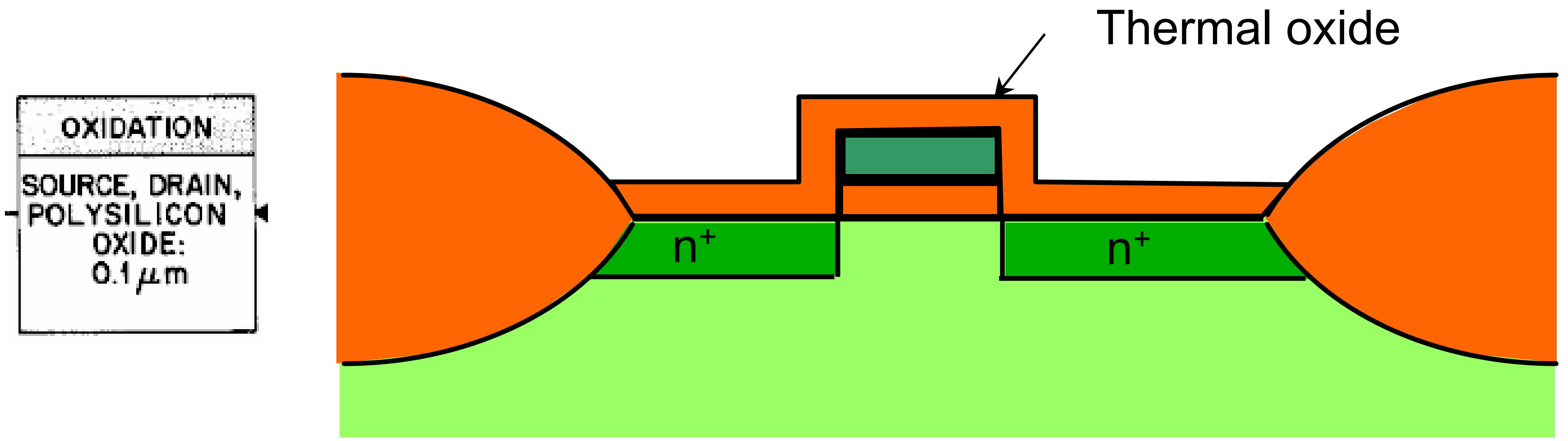
As+ 80keV, 10^{16}/cm^2

ION IMPLANT

SOURCE/DRAIN: 1×10^{16} As/cm^2, 80keV

Resist

n^+ n^+



DEPOSITION

SPUTTER Aℓ METALLIZATION: 0.7 µm

Al

CVD oxide

intermediate oxide

n^+ n^+

ANNEAL

HYDROGEN ANNEAL

H_2 anneal
~ 400°C