Process Integration

Self-aligned Techniques
• LOCOS- self-aligned channel stop
• Self-aligned Source/Drain
• Lightly Doped Drain (LDD)
• Self-aligned silicide (SALICIDE)
• Self-aligned oxide gap

MEMS Release Techniques
• Sacrificial Layer Removal
• Substrate Undercut

Example IC Process Flows
• NMOS - Generic NMOS Process Flow
• CMOS - The MOSIS Process Flow

Advance MOS Techniques
• Twin Well CMOS, Retrograde Wells, SOI CMOS
Self-aligned channel stop with Local Oxidation (LOCOS)

LOCOS Process Flow

Si₃N₄ CVD
pad oxide

Si
B⁺ channel stop implant

Si

dose
~10^{13}/cm²

thermal oxidation (high temperature)

Self-aligned channel stop
Comment: Channel Inversion

If poly or metal lines lie on top of the FOX, they will form a parasitic MOS structure. If these lines carrying a high voltage, they may create an inversion layer of free electrons at the Si substrate and shorts out neighboring devices. The relatively highly doped Si underneath (the “channel stop”) raises the threshold voltage needed for the inversion.
Comments: Non self-aligned alternative:

Disadvantages:
1. Two lithography steps
2. Channel stop doping not FOX aligned
Self-aligned Source and Drain

* The n+ S/D always follows gate
Comment: Non self-aligned Alternative

1. Solution: Use gate overlap to avoid offset error.

2. Channel not linked to S/D

Disadvantages: Two lithography steps, excess gate overlap capacitance
Lightly Doped Drain (LDD)
Lightly Doped Source/Drain MOSFET (LDD)

The n-pockets (LDD) doped to medium conc (~1E18) are used to smear out the strong E-field between the channel and heavily doped n+ S/D, in order to reduce hot-carrier generation.
LDD Process Flow using Ion Implantation

n implant for LDD

CVD conformal deposition SiO₂

Directional RIE of CVD Oxide
Spacer left when CVD SiO₂ is just cleared on flat region.

0.25μm

0.05μm

n⁺ implant

n⁺ n n n⁺ n
Self-Aligned Silicide Process (SALICIDE) using Ion Implantation and Metal-Si reaction

Metal silicides are metallic. They lower the sheet resistance of S/D and the poly-gate.
SALICIDE Process Flow

oxide spacer

\[
\text{SiO}_2
\]
Ti deposition

$\text{Ti} + 2\text{Si} \rightarrow \text{TiSi}_2$

$\text{Ti}$ will not react with $\text{SiO}_2$.

Selective etch to remove unreacted $\text{Ti}$ only.
Self-aligned Oxide Gap

DRAM structure (MOSFET with a capacitor)

For a small spacing between poly-I and poly-II, inversion charges between MOSFET and Capacitor are electrically linked. No need for a separate n+ island.
Process Flow of MEMS Rotating Mechanisms

In-Plane Movement

Micro-turbine Engine
Process Flow for a Hinge Structure

Out-of-plane Movement

- Poly - 1
- Poly - 2
- Contact

Silicon

Poly - 1

PSG

Hinge Pin

Staple

Plate

Poly - 2

Hinge Plate

Plate

Staple
Layout of Thermal Bimorph Actuator

(See 143 Lab Manual for details)
After Patterning Poly-Si (Mask #2)

Top View

Cross Section

- Aluminum
- Poly Si
- Oxide
- Si substrate
- Al-Poly contact
After Patterning Intermediate Oxide (Mask #3, Contact-Hole Cut)

**Top View**

- Aluminum
- Poly Si
- Oxide
- Si substrate
- Al-Poly contact

**Cross Section**
After Aluminum patterning (Mask #4)

To contact pad

Top View

Cross Section

- Aluminum
- Poly Si
- Oxide
- Si substrate
- Al-Poly contact
After XeF2 selective etching of Si Substrate (Final Structure)
A Generic NMOS Process Flow

Substrate
Boron doped (100)Si
Resistivity = 20 Ω-cm

Thermal Oxidation
~100 Å pad oxide

CVD Si₃N₄
~ 0.1 um

Lithography
Pattern Field Oxide Regions

RIE removal of Nitride and pad oxide

Channel Stop Implant:
3x10¹² B/cm² 60keV

Thermal Oxidation to grow 0.45 µm oxide

Wet Etch Nitride and pad oxide

Ion Implant for Threshold Voltage control
8x10¹¹ B/cm² 35keV

Thermal Oxidation To grow 250 Å gate oxide

LPCVD Poly-Si
~ 0.35um

Dope Poly-Si to n+ with Phosphorus Diffusion source
A Generic NMOS Process Flow (cont.)

1. **Lithography**
   - Poly-Si Gate pattern
   - RIE Poly-Si gate
   - Source /Drain Implantation ~ $10^{16}$ As/cm$^2$ 80keV

2. **Thermal Oxidation**
   - Grow ~0.1um oxide on poly-Si and source/drain
   - LPCVD SiO2 ~0.35um
   - Lithography Contact Window pattern

3. **RIE removal of CVD oxide and thermal oxide**
   - Sputter Deposit Al metal ~0.7um
   - Lithography Al interconnect pattern

4. **RIE etch of Al metallization**
   - Sintering at ~400°C in H2 ambient to improve contact resistance and to reduce oxide interface charge
NMOS Structure

Generic NMOS Process Flow

Boron-doped Si
20 $\Omega$-cm
$<100>$

device active

$\sim 5 \mu m$

$500 \mu m$

$p$-type substrate
ETCH
DRY ETCH:
NITRIDE/PAD
OXIDE

ION IMPLANT
CHAN-STOP:
3\times 10^{12} \text{B/cm}^2,
60\text{keV}

P.R.

SiO_2

nitride

Si

P.R.

SiO_2

nitride

Si

B: 3 \times 10^{12} / \text{cm}^2
60\text{keV}

0.1\mu\text{m}

3 \times 10^{17} / \text{cm}^3
$p^+ p^+$

$35/105 \times 211$ 

$B \times 10^{11}/cm^2 35keV$
As+ 80keV, $10^{16}$/cm$^2$

Thermal oxide

Ion implant:
- Source/Drain: $1 \times 10^{16}$ As/cm$^2$, 80keV

Oxidation:
- Source, Drain, Polysilicon Oxide: 0.1 μm
$\text{H}_2$ anneal
$\sim 400^\circ\text{C}$

$\text{DEPOSITION}$
$\text{SPUTTER A}_{\text{L}}$
$\text{METALLIZATION: 0.7} \mu\text{m}$

$\text{ANNEL}$
$\text{HYDROGEN ANNEAL}$

Intermediate oxide

Al

CVD oxide

$n^+$

Si/SiO$_2$

Interface States Passivation