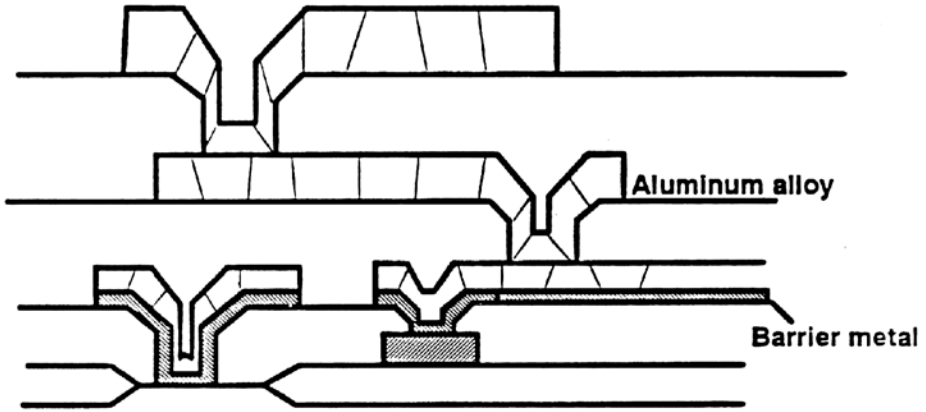
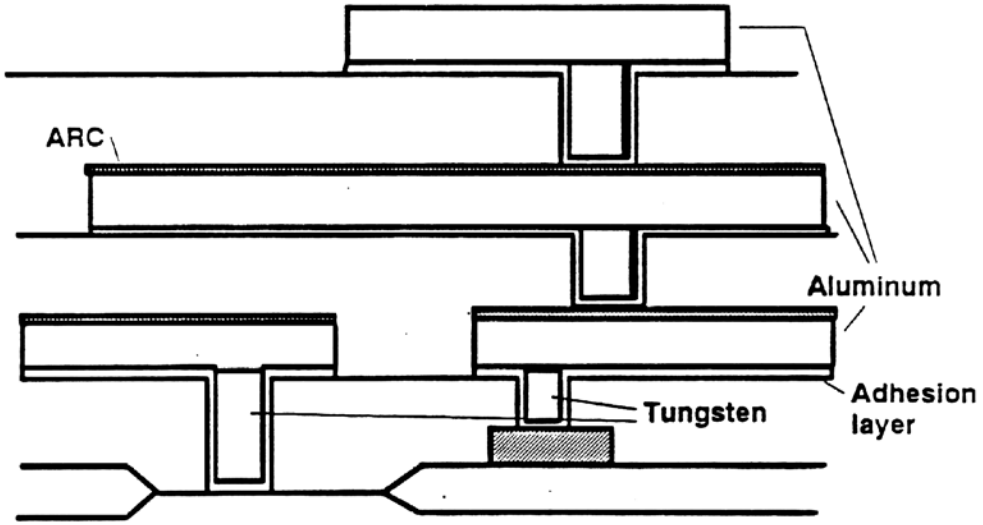
MULTILEVEL INTERCONNECT STRUCTURES



Non planar multilevel interconnect structure

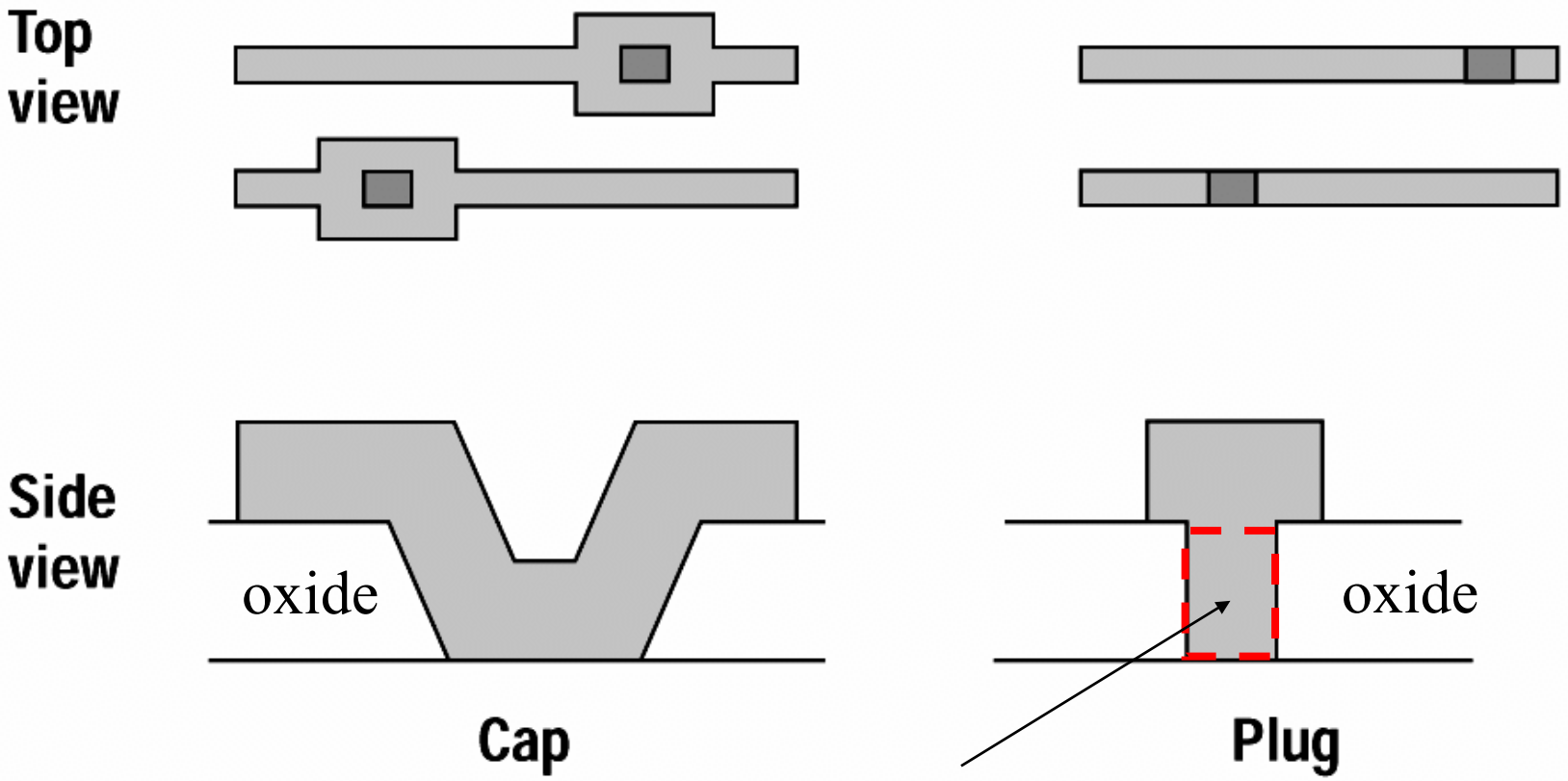
Nonplanar Metallization



Planar multilevel interconnect structure

Planar Metallization

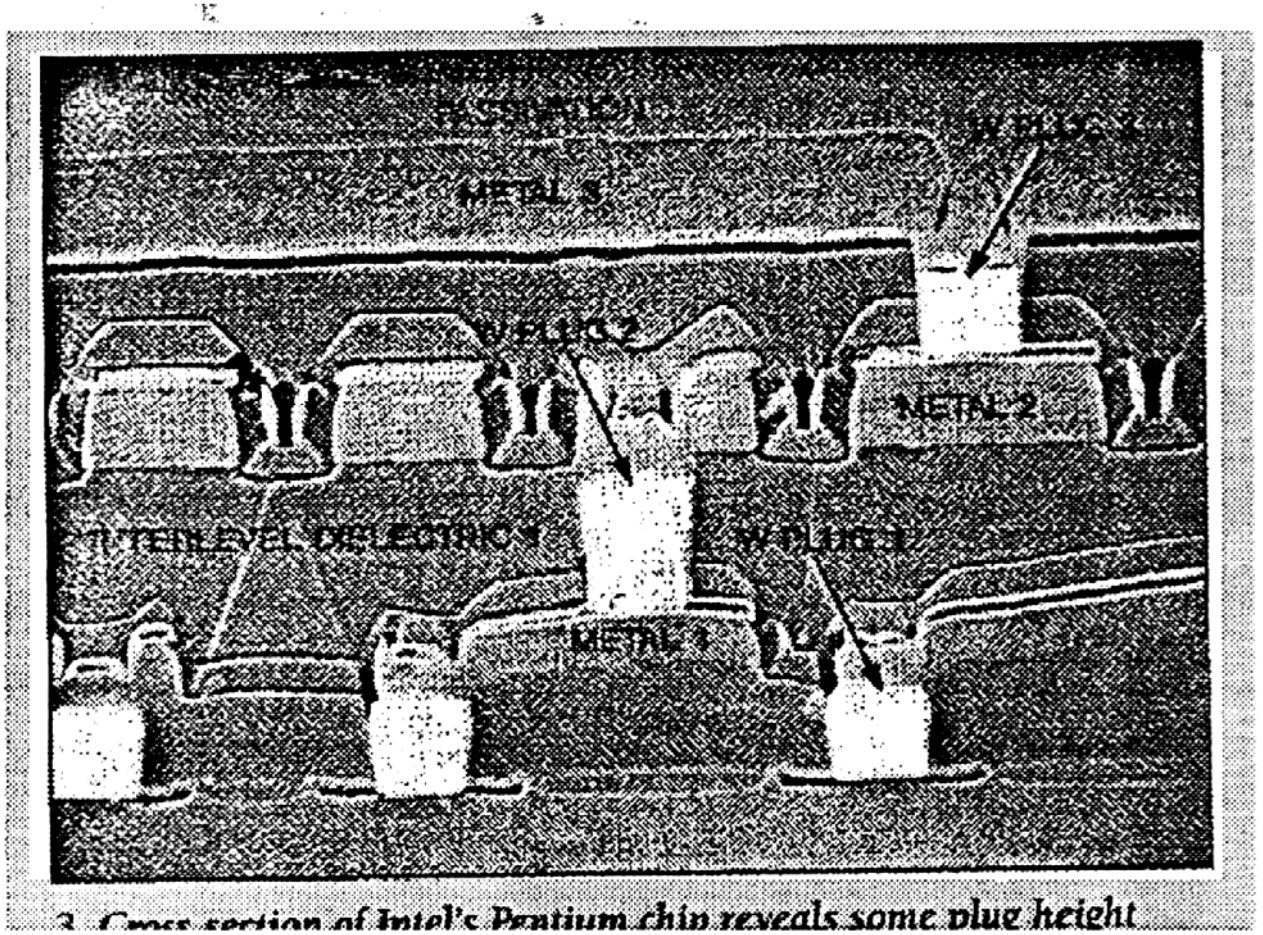
"Caps" and "Plugs"



The plug material can be same as interconnect material (e.g. Cu) or different material (e.g. W)

Figure 13.22 The use of caps versus plug-filled contacts.

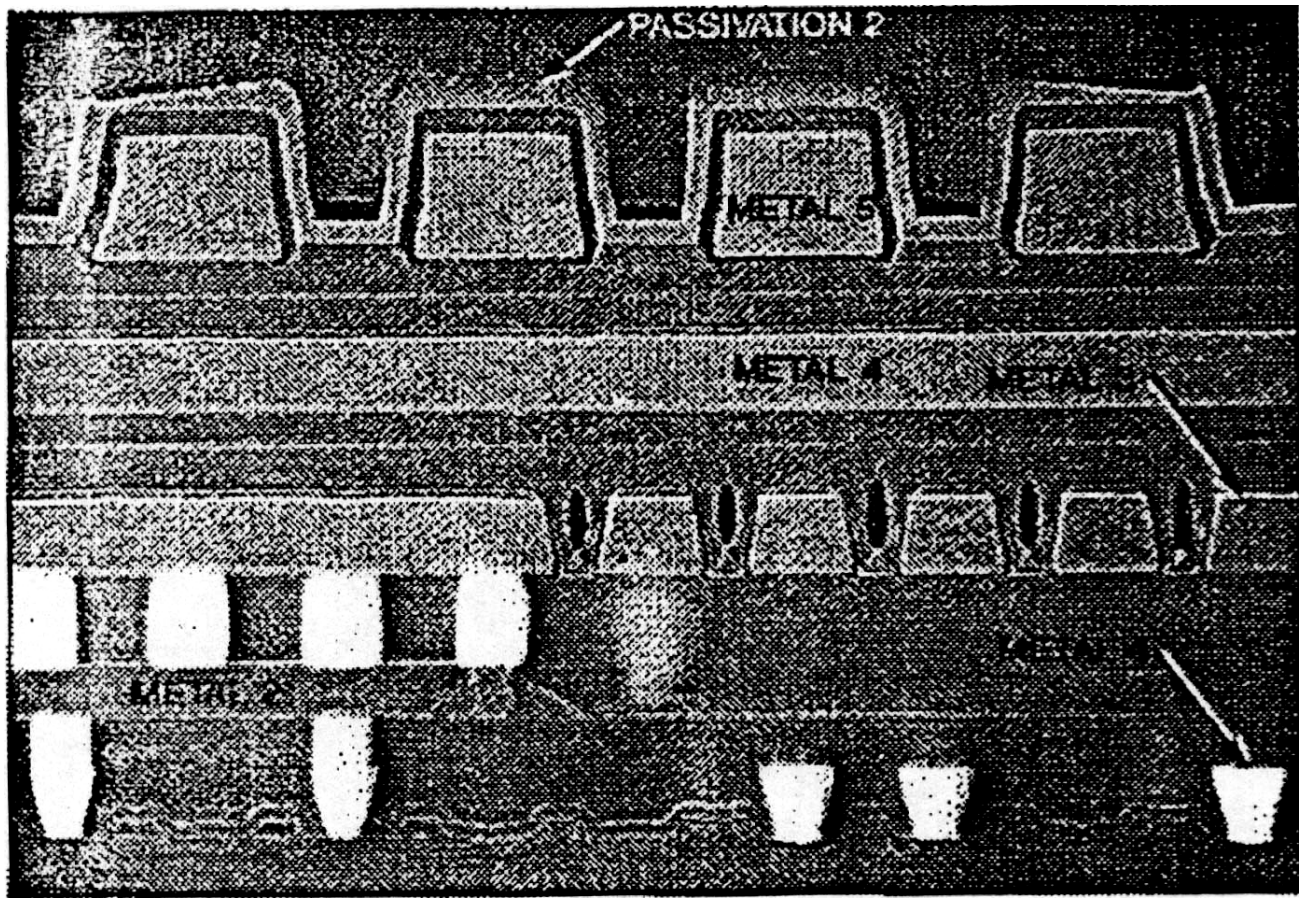
Non-Optimized Planarization example



3. Cross section of Intel's Pentium chip reveals some plug height

THREE LEVEL METALLIZATION FROM COMPANY A
W plugs for contacts, via 1 and via 2
Al/TiN/Ti/TiN for metal 1 and 2; Al alloy for metal 3
CMP for IMO 1 and IMO2 .

Good Planarization Example

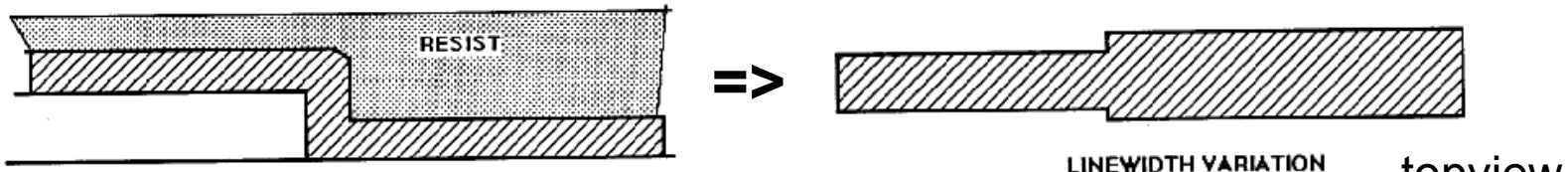


Five Level Metallization for Company C
W plugs for contacts and vias
W for metal 1, Al/Ti metal 2,3, 4; Al metal 3
CMP for all dielectrics.

Surface Planarization

Benefits for Lithography Processes:

- Lower Depth-of-Focus requirement
- Reduced optical reflection effects on resist profiles
- Reduced resist thickness variation over steps

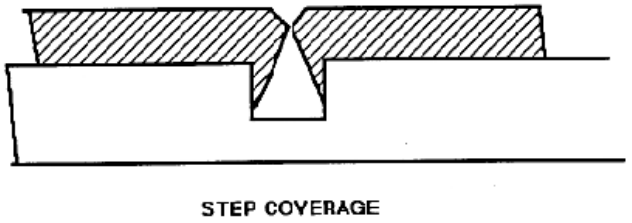


Benefit for Etching Processes:

- Reduced over-etch time required due to steps

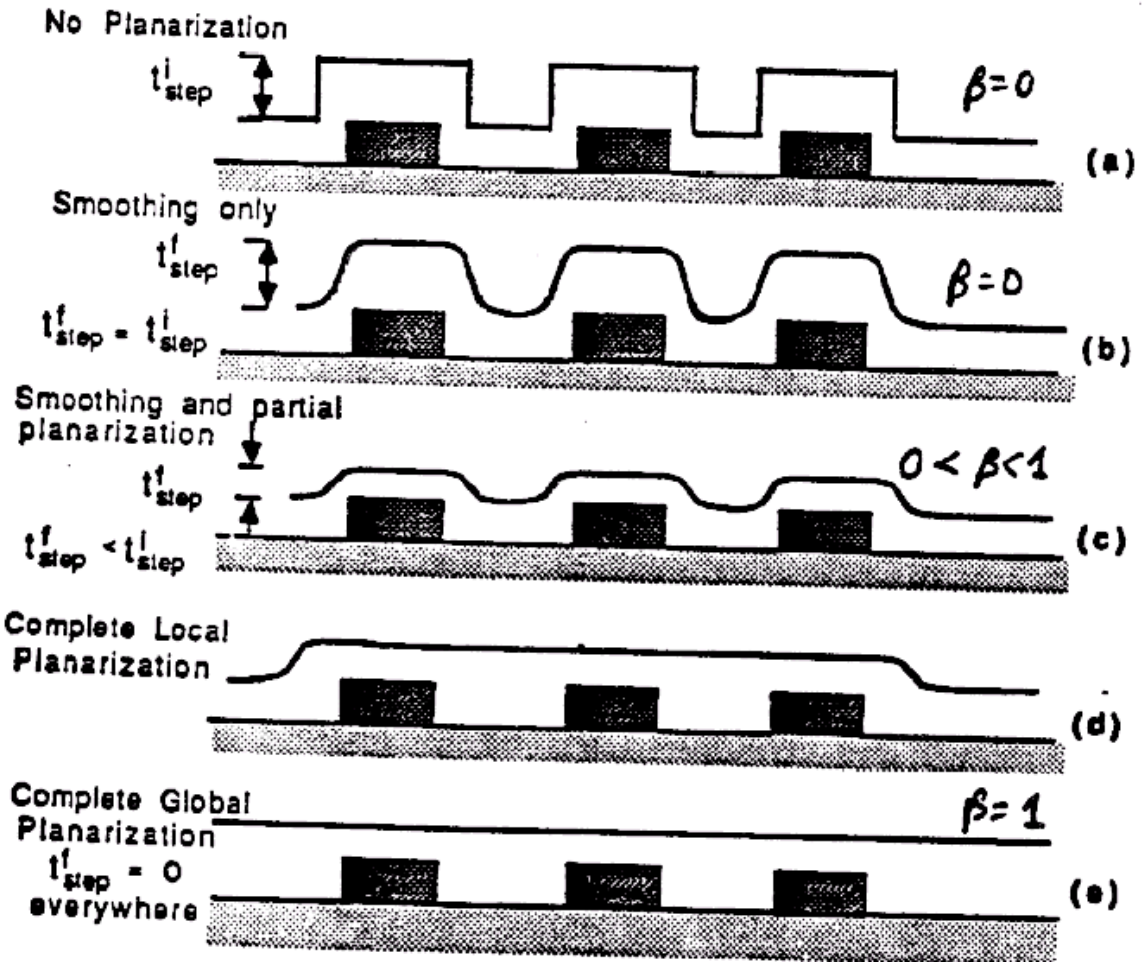
Benefit for Deposition Processes:

- Improved step coverage for subsequent layer deposition

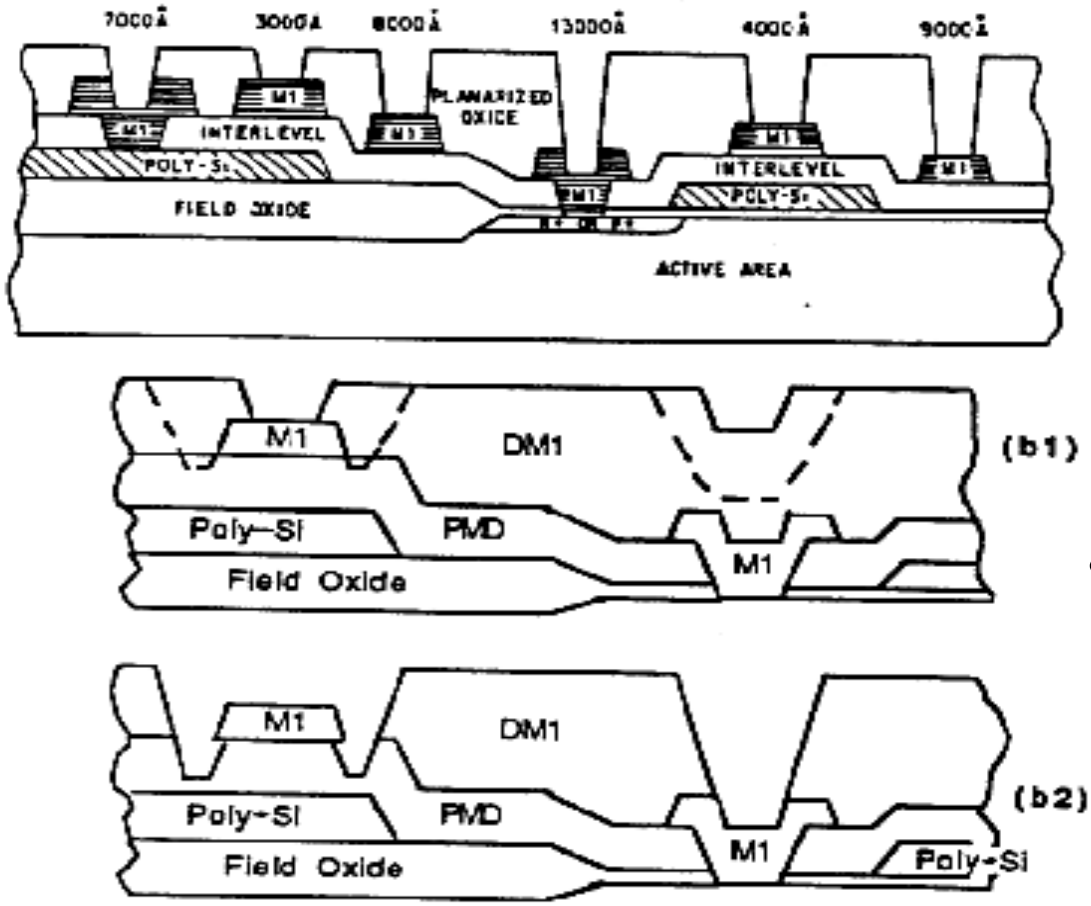


Planarization Factor β

$\beta = 1 - (\text{final step height/initial step height})$



Planarization: A bad example



- **Topography management must start at lower layers!**

Fig. 4-13 (a) Example which shows how much the via depth can vary in a DLM process if full planarization is achieved.[259] (© 1985 IEEE). (b) If a sloped-sidewall etch is used to etch the vias shown in part (a), the dimensions of the shallow vias will continue to increase during the time needed to completely etch the deep vias. If the lateral dimensions of the shallow vias exceed the width of the Metal 1 pattern below these vias, the etch process will begin to erode the PMD layer (b2), even if a nested via is used.

Planarization Techniques

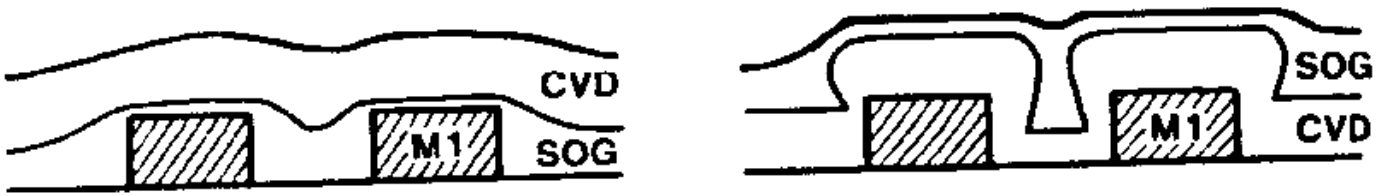
1. Spin-on glass or polyimide

2. Deposit and Etchback

3. Chemical-Mechanical Polishing (CMP)

Spin-On Glass (SOG)

A: SOG STANDALONE



B: CVD/SOG COMPOSITE

C: CVD/SOG/CVD COMPOSITE
WITH PARTIAL SOG ETCH-BACK

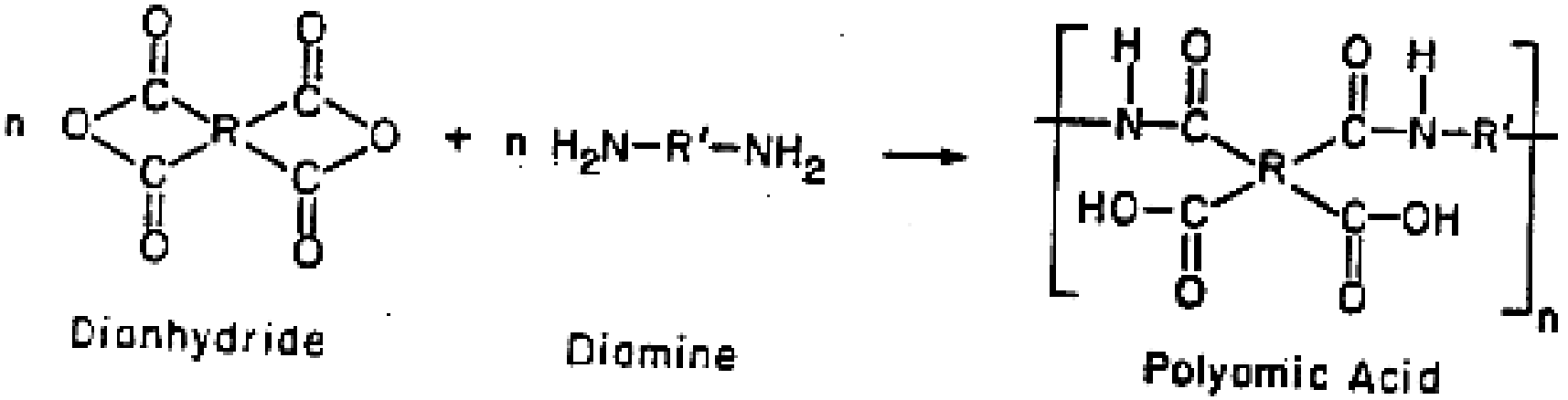
SOG Annealing

- Cure:
- 400-500°C -> inorganic backbone polymer
  - exact composition depends on SOG type
- 800-1100°C -> densified glass (inorganic SOGs)
- can be performed in N_2, O_2 or steam
  - steam allows densification to occur at lower
  - temperatures

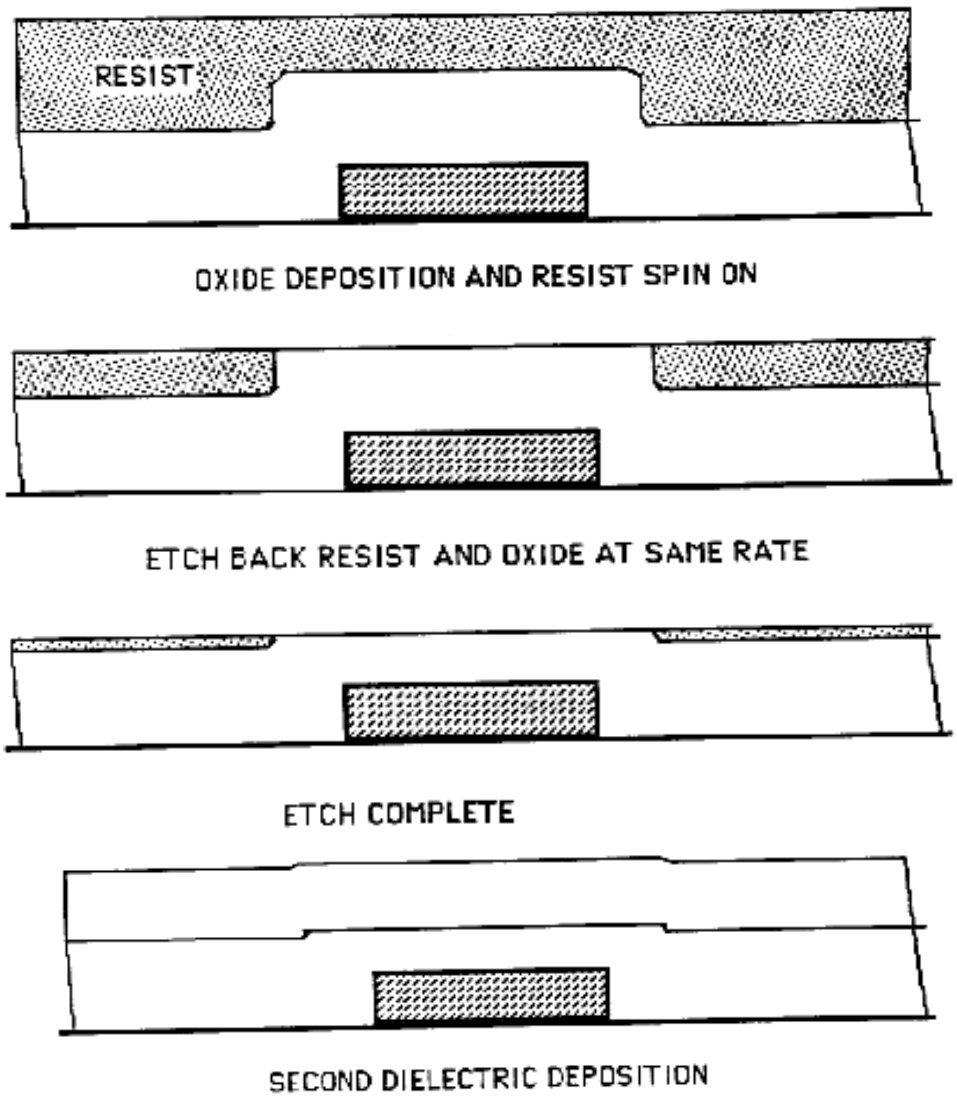
Polyimides

Polymers:

- excellent thermal stability (up to 450°C)
- good dielectric properties (ε_r=3.3, ρ=10^{16} Ω-cm)
- superior chemical resistance



Deposit and Etchback



1. Deposit thick oxide layer (600 - 1000nm)
2. Spin on resist or polymer to planarize surface
3. Etch back with a process that has equal oxide and resist/polymer etch rates (e.g. $CF_4 + O_2$ dry etch)

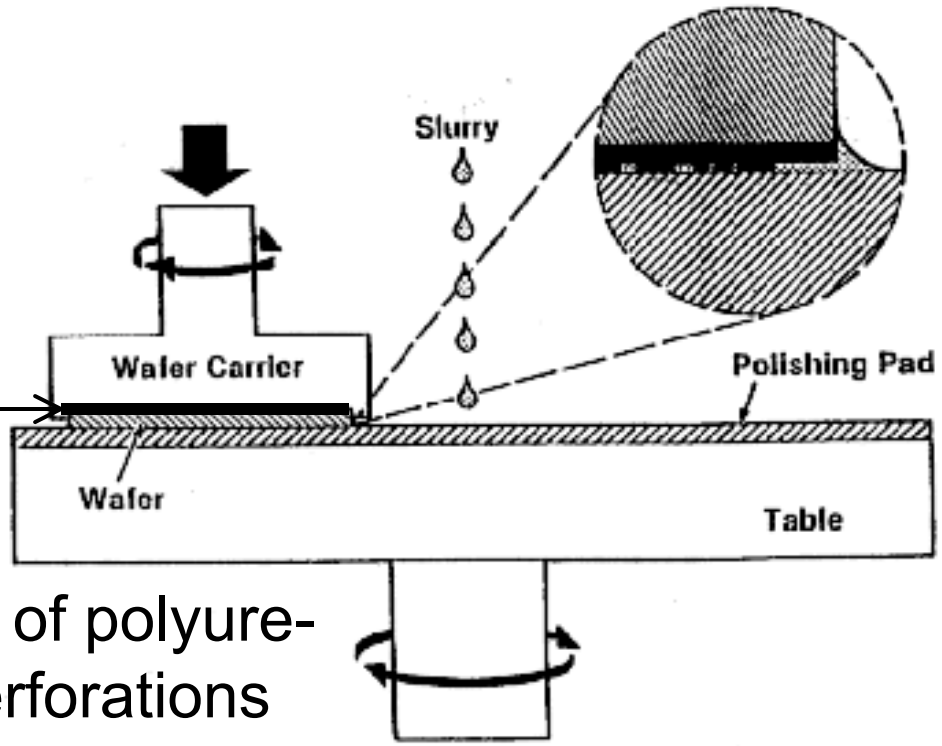
(4. Deposit second oxide layer)

- Simple process, requiring equipment and materials already available in the lab

Chemical Mechanical Polishing (CMP)

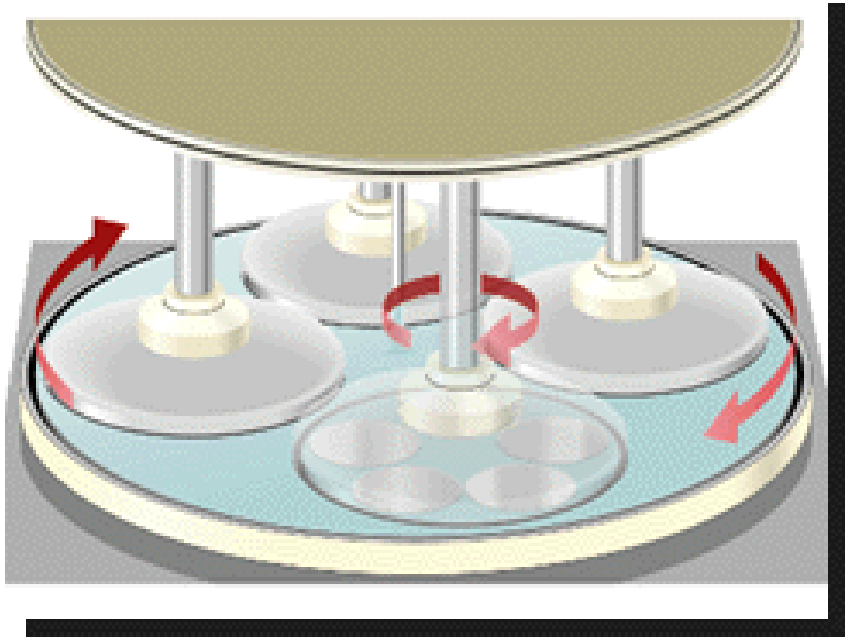
Wafer is polished using a slurry containing
- silica abrasives (10-90 nm particle size)
- etching agents (e.g. dilute HF)

- Backing film provides elasticity between carrier and wafer

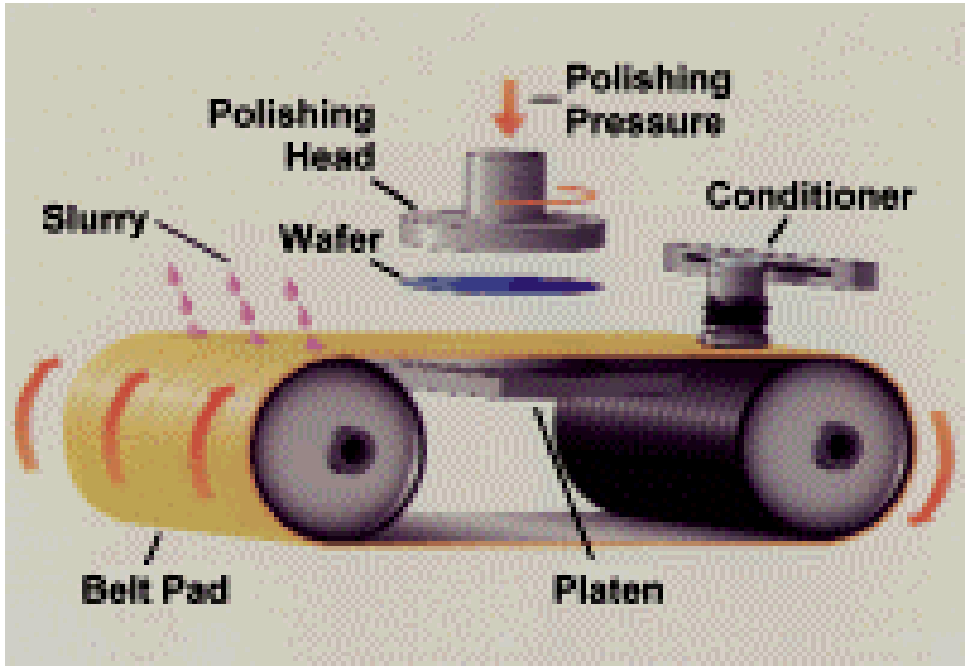


- Polishing pad made of polyurethane, with 1 mm perforations
  - rough surface to hold slurry

CMP Configurations

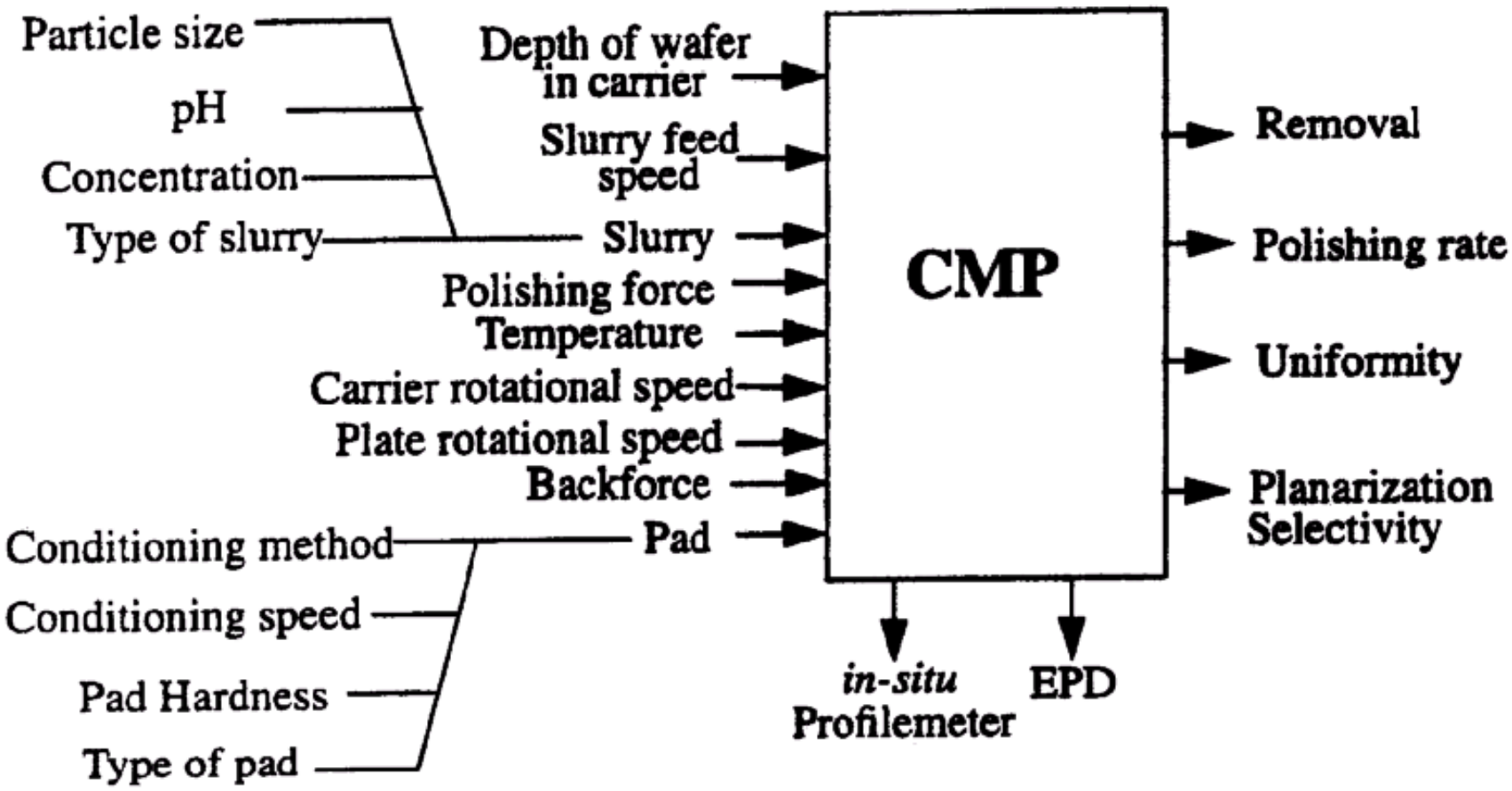


Rotating wafer
Rotating pad



Rotating Wafer
Linear track pad

CMP Process Control



For reference only

CMP Rate

Preston Model:

Local Removal rate $R = K_p P v$

where P = local applied pressure

v = *relative* pad-wafer velocity

K_p = Preston coefficient [unit in pressure^{-1}]

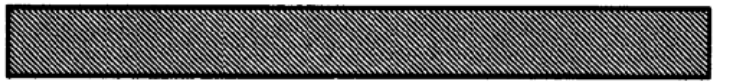
function of film hardness, Young's modulus,
slurry, pad composition and structure

CMP Selectivity

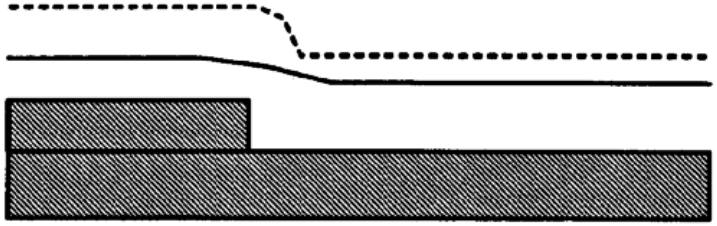
CMP of	Selectivity to Si_3N_4
SiO_2	6:1
poly-Si	280:1
W	75:1
Al	40:1

Problems encountered in CMP

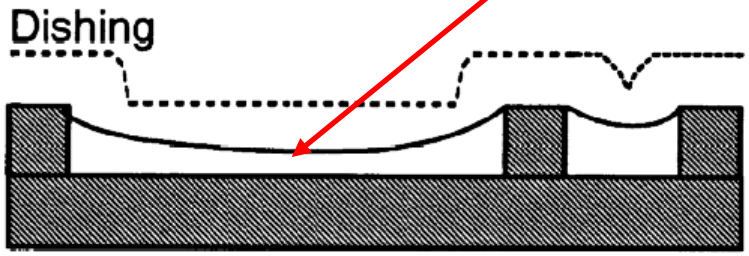
Non uniformity



Rounding



Dishing



Pattern dependence

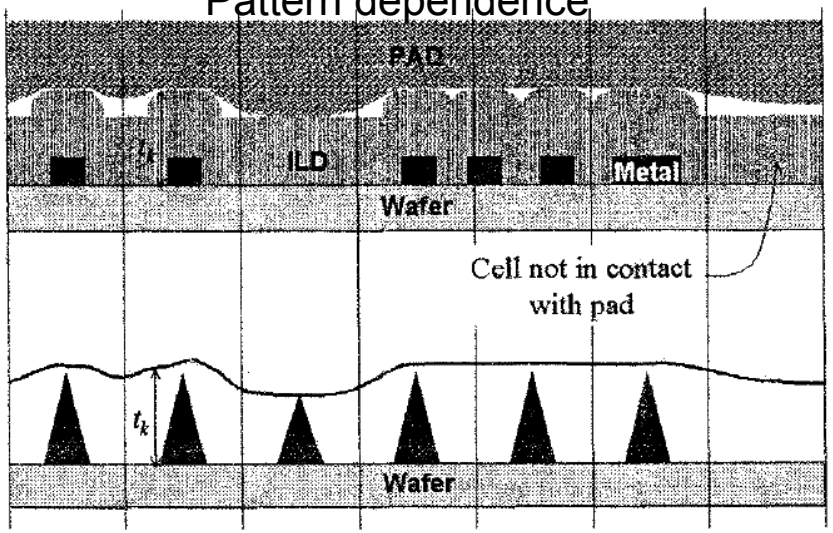
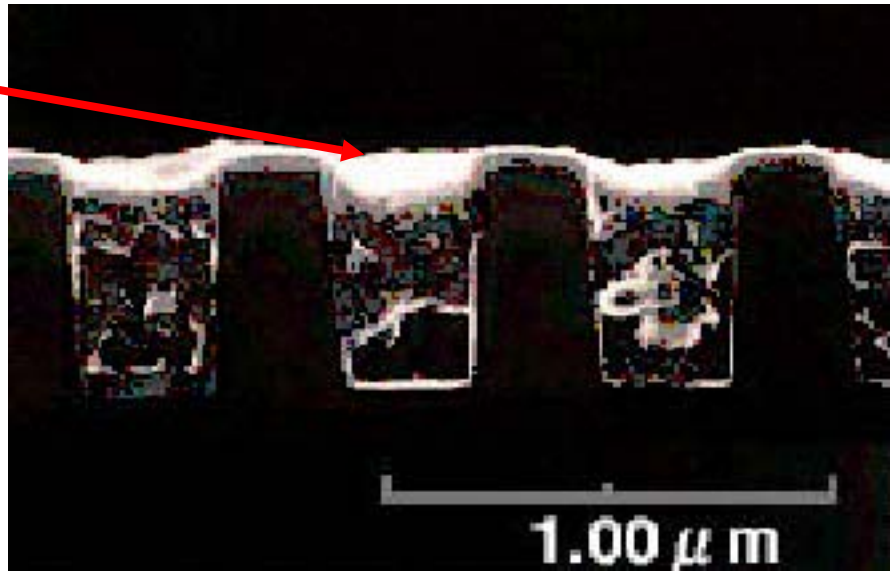


Fig. 6. Mechanical model (with exaggerated pad bending).



Pattern Dependence of CMP

***Note :Y-axis highly magnified !!!**

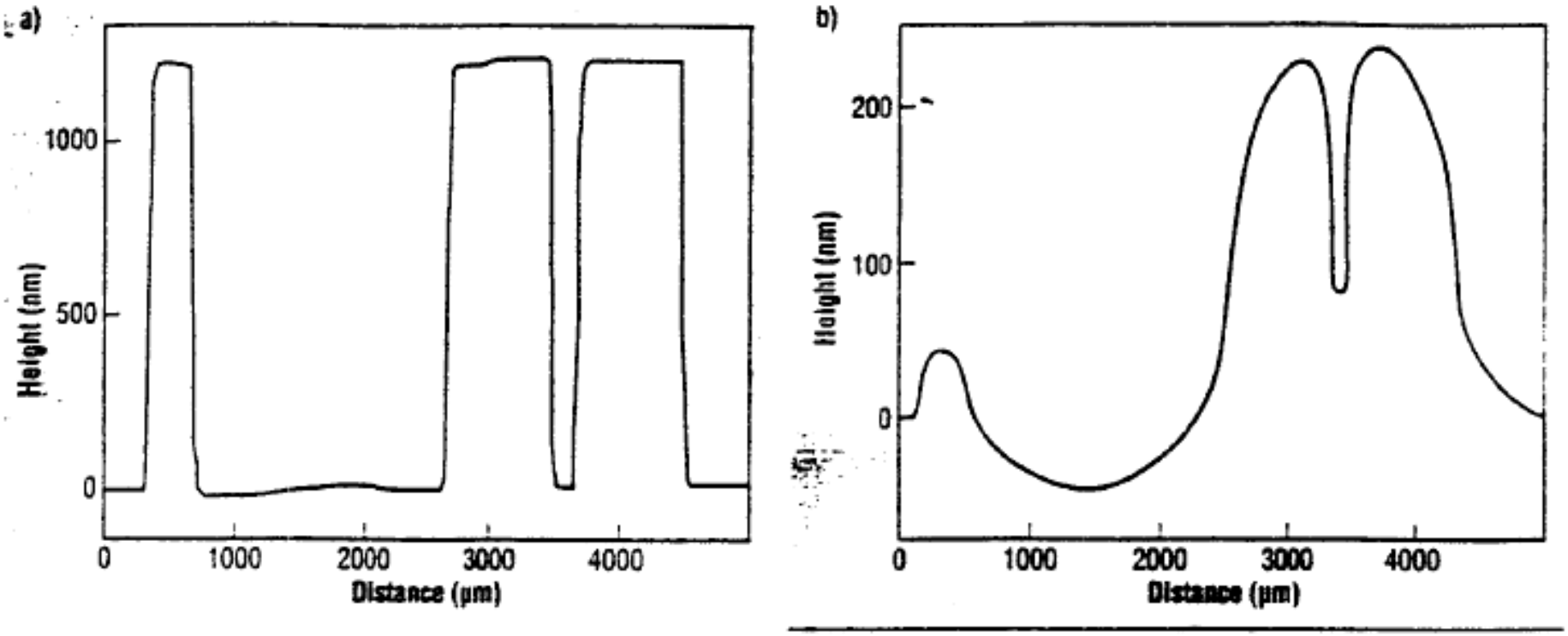


Figure 7. Polishing test structure (a) prior to polishing and (b) after 4 minutes of polishing

- High isolated features polish fast
- Increased pressure at corners of features creates rounding

CMP Endpoint Detection - (1) Polisher Motor Current

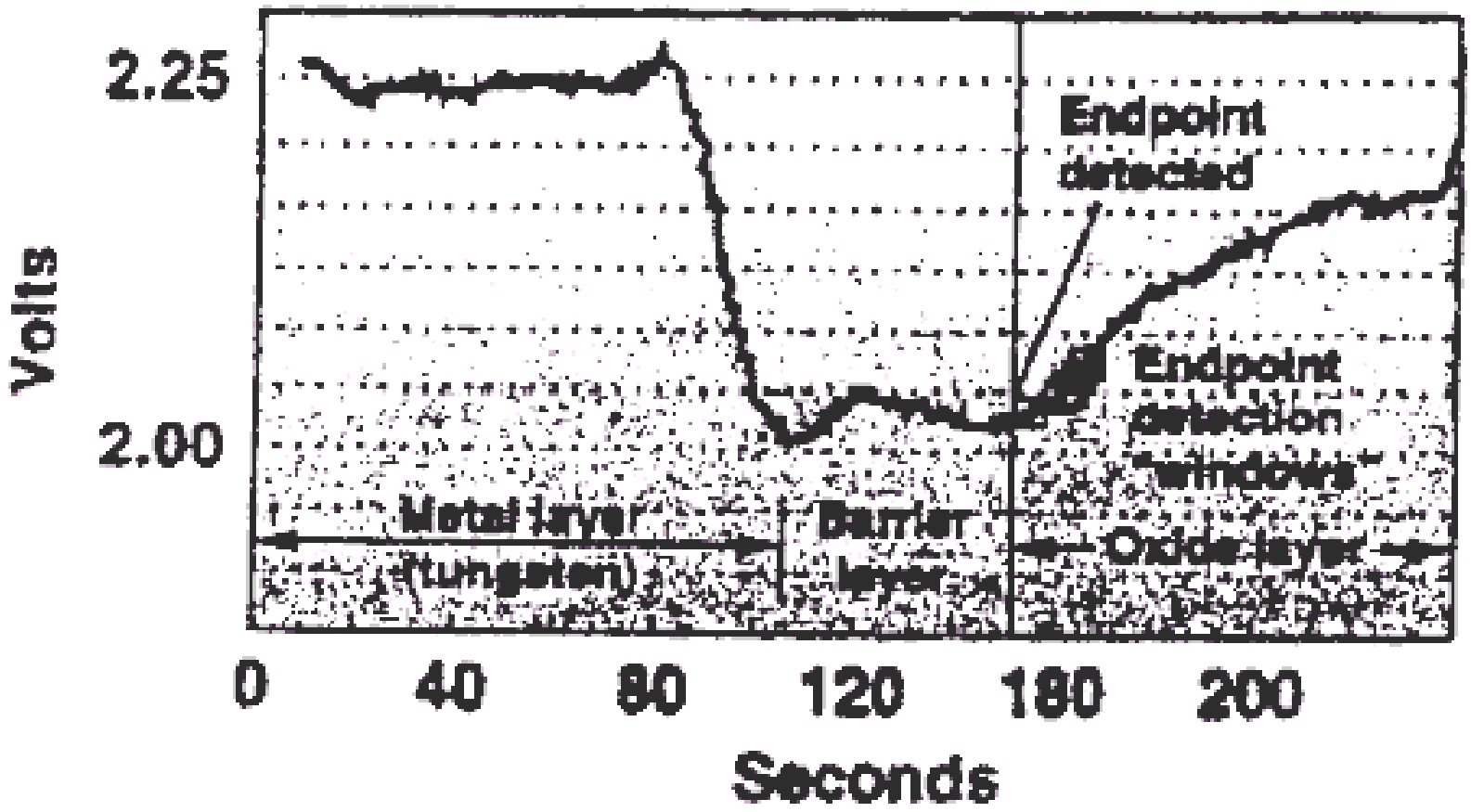


Figure 12. End-point detection using wafer carrier motor current (source 20).

CMP Endpoint Detection - (2) Optical Interference

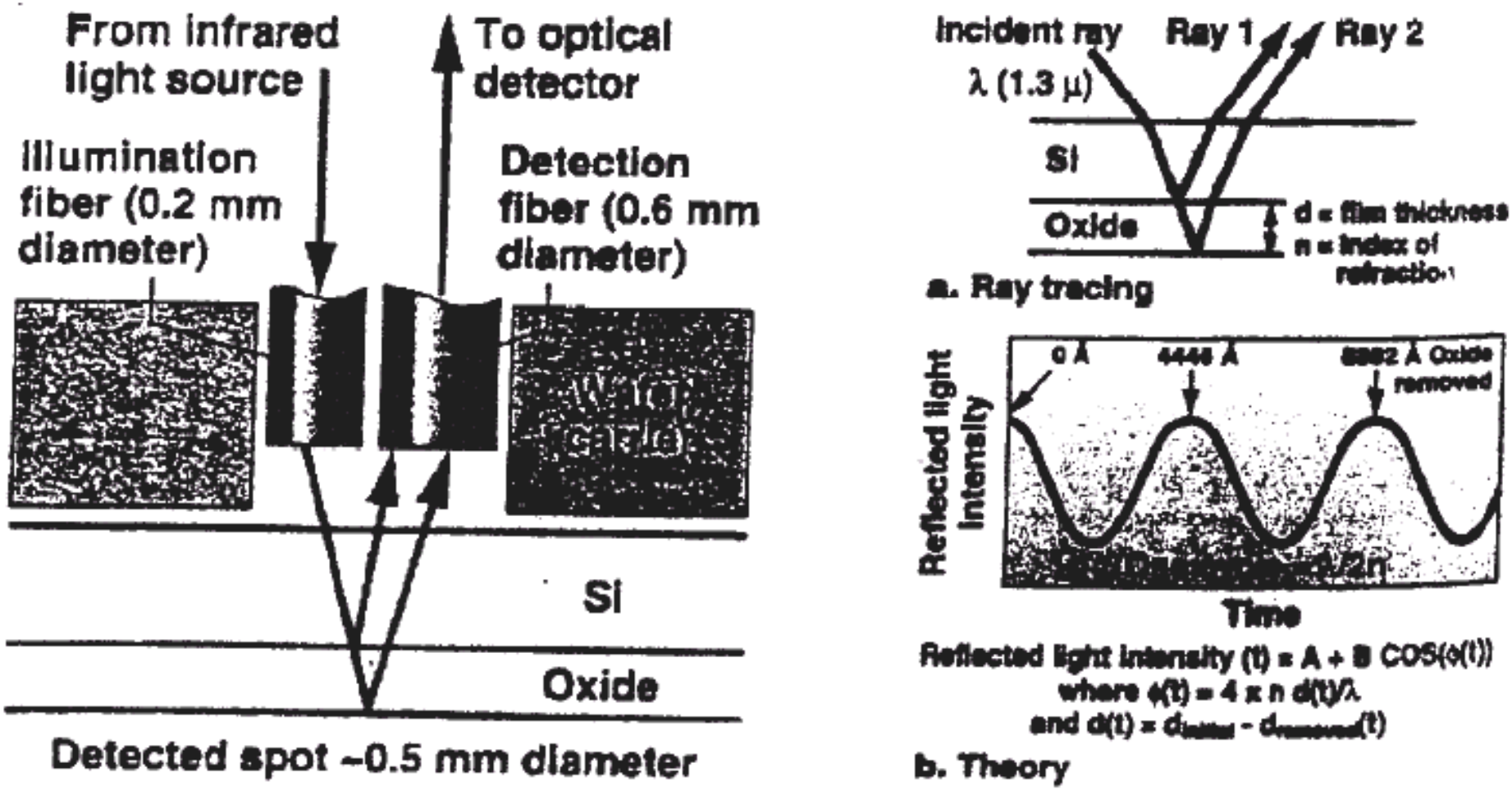


Figure 13. Diagram of a IR sensor embedded into the wafer carrier (left). Description of IR interferometry using the IR sensor (right) (source 20).

CMP Application Example

RIE of Cu difficult due to low vapor pressure of by-products

=> Cu lines formed by CMP

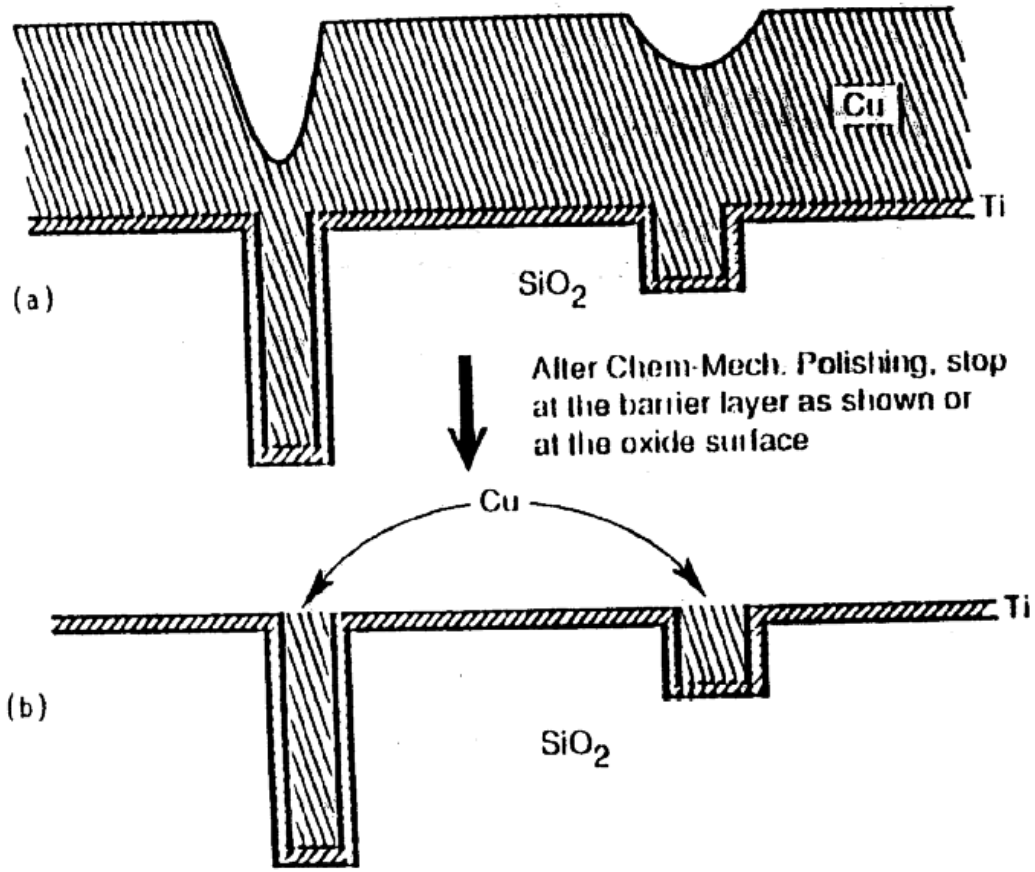


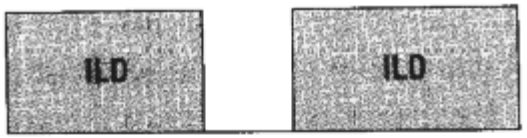
Figure 2. Schematics of the inlaid Cu produced by chemical-mechanical polishing (CMP): (a) shows a deposited Cu/Ti on patterned dielectric, (b) the same after CMP and stopping at Ti.

Cu has to be
encapsulated
by a liner (e.g. TiN)
to prevent out-diffusion
into SiO2 and Si

Single Damascene Process

ILD = Inter-Level Dielectric

1



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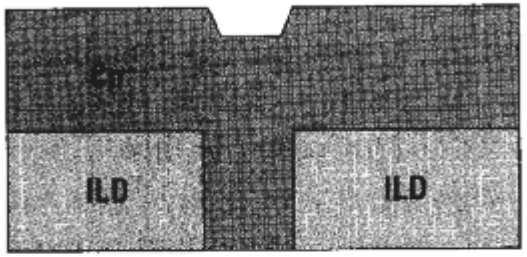

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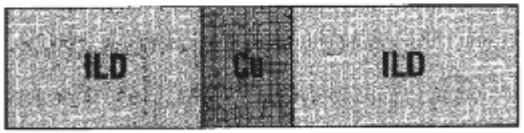

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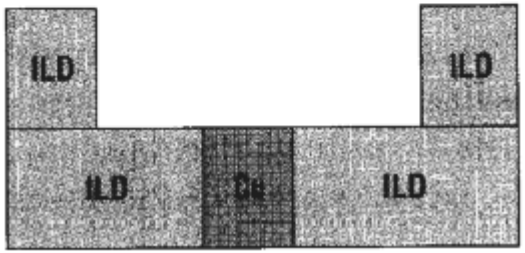

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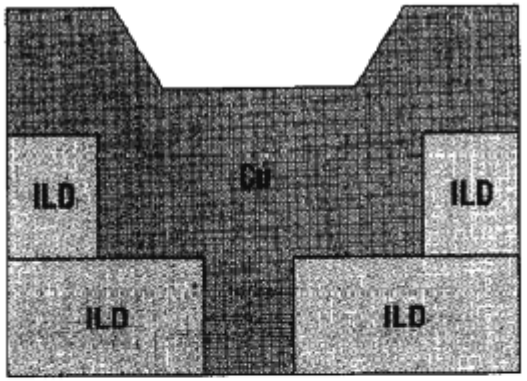

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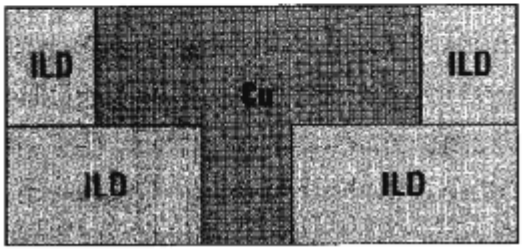
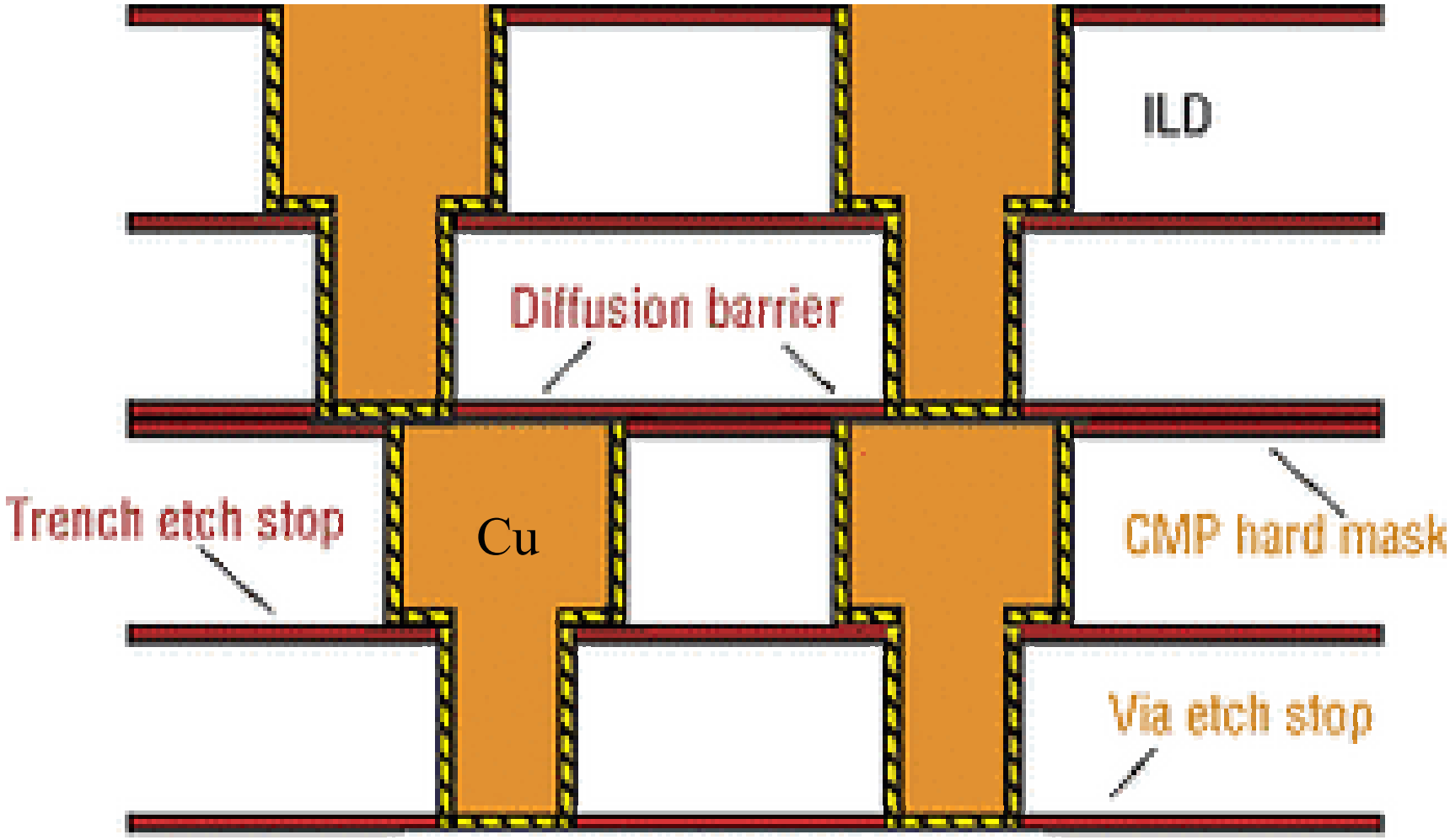
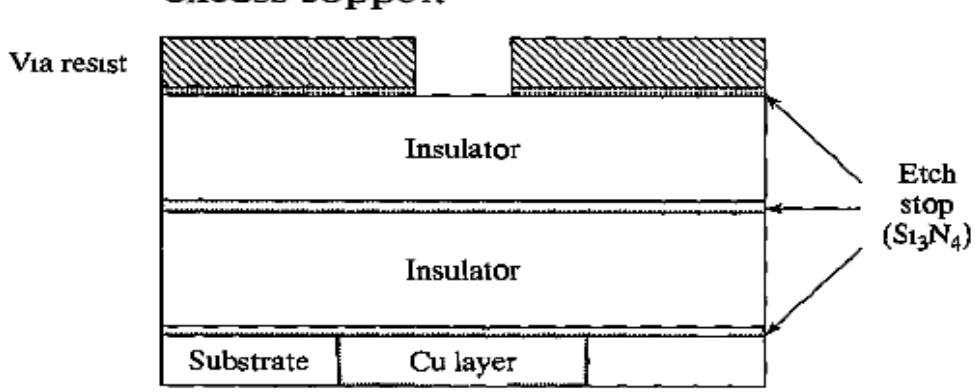


Dual Damascene Cu Metallization with Diffusion Barrier

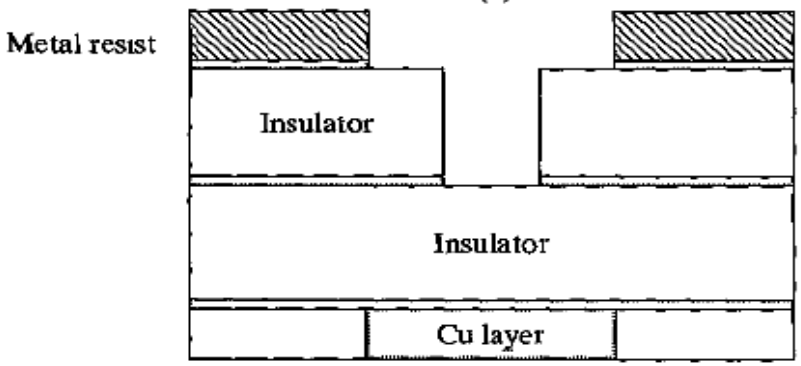


Dual Damascene Process Sequence

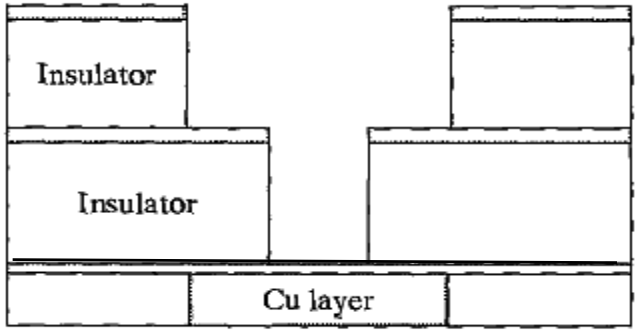
Dual Damascene process flow (a) An insulator sandwich is first deposited and the upper nitride layer is patterned. The insulator layer is etched The etch terminates on the silicon nitride etch stop. (b) The nitride layer is patterned and etched. (c) Following the next oxide etch step, two different width openings exist in the two oxide layers. (d) Barrier and seed layers are deposited and plated with copper. (e) Final structure following removal of excess copper.



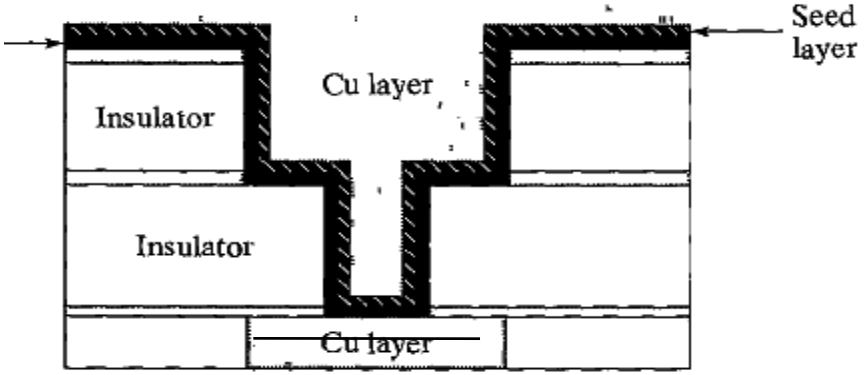
(a)



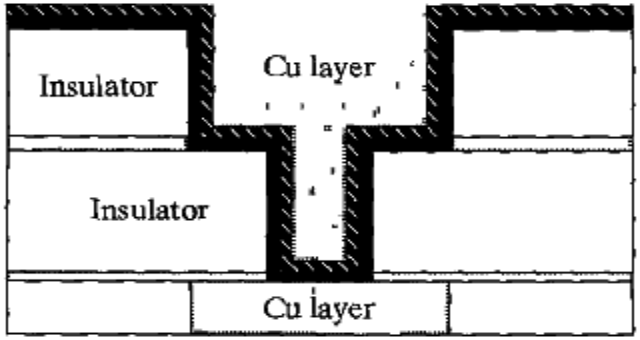
(b)



(c)



(d)



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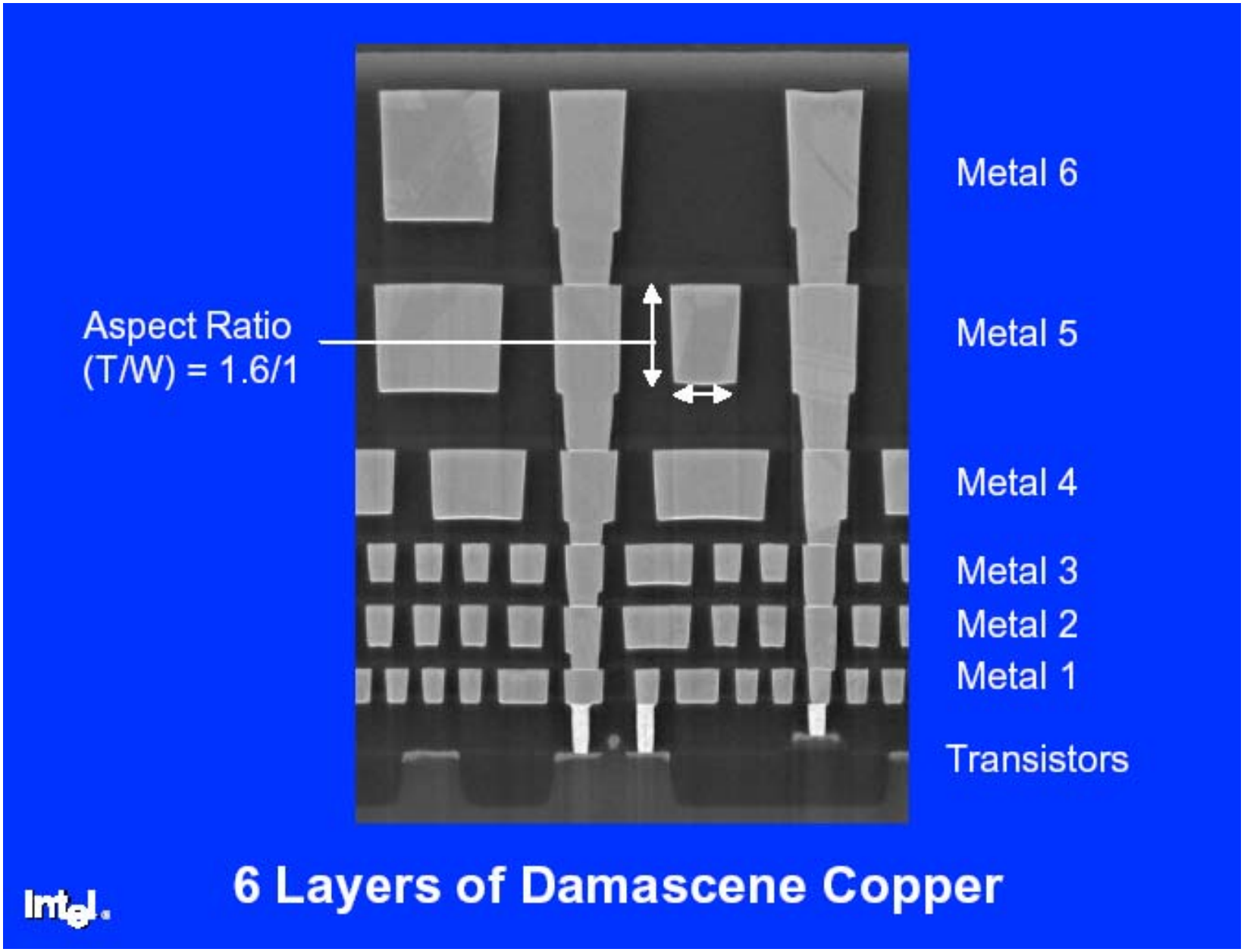
Aspect Ratio
(T/W) = 1.6/1
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Transistors
6 Layers of Damascene Copper
Intel