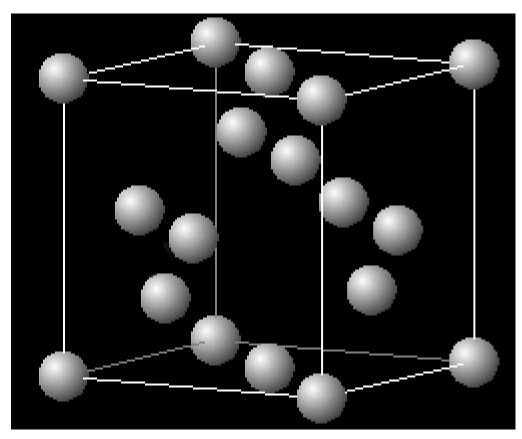
Crystallographic Planes

Unit cell:

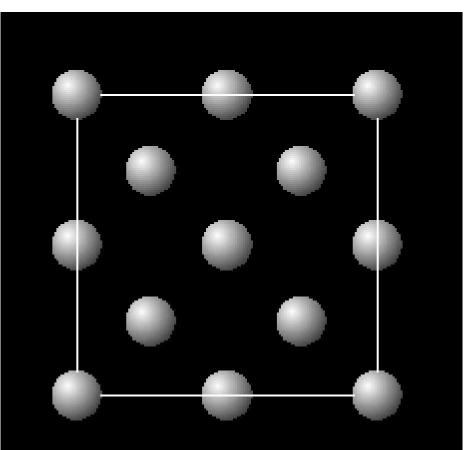


Si lattice constant =

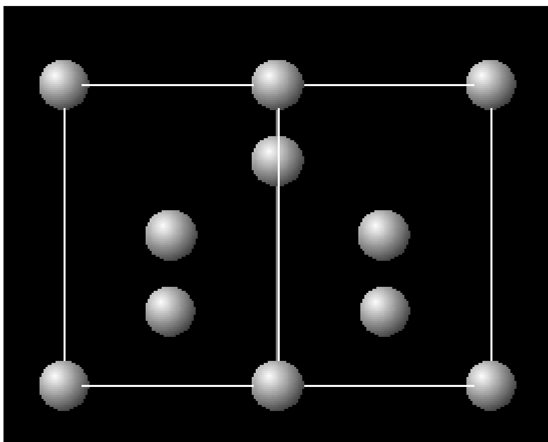
5.431Å

→ 5 x 10^{22} atoms/cm^3

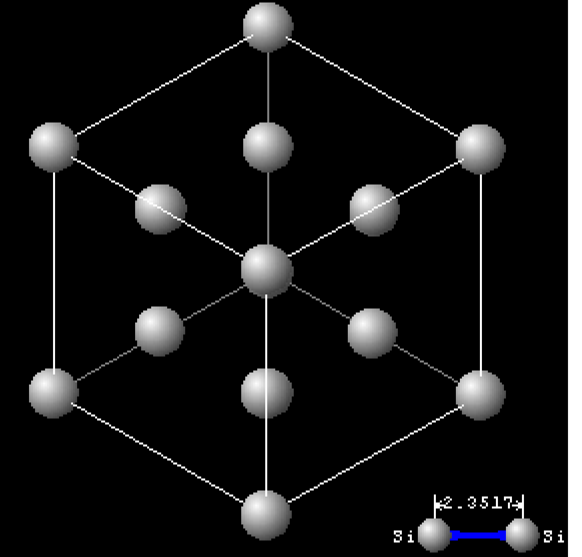
View in <100> direction



View in <110> direction

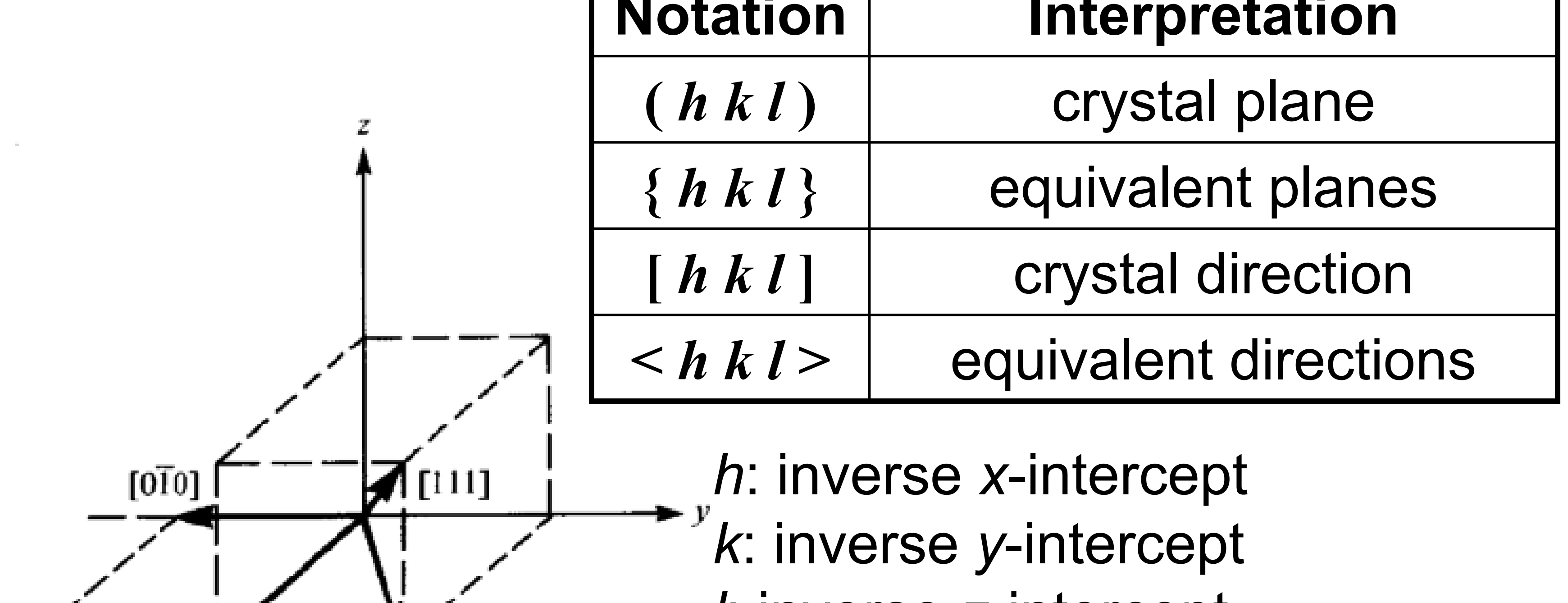


View in <111> direction



Crystallographic Notation

Miller Indices



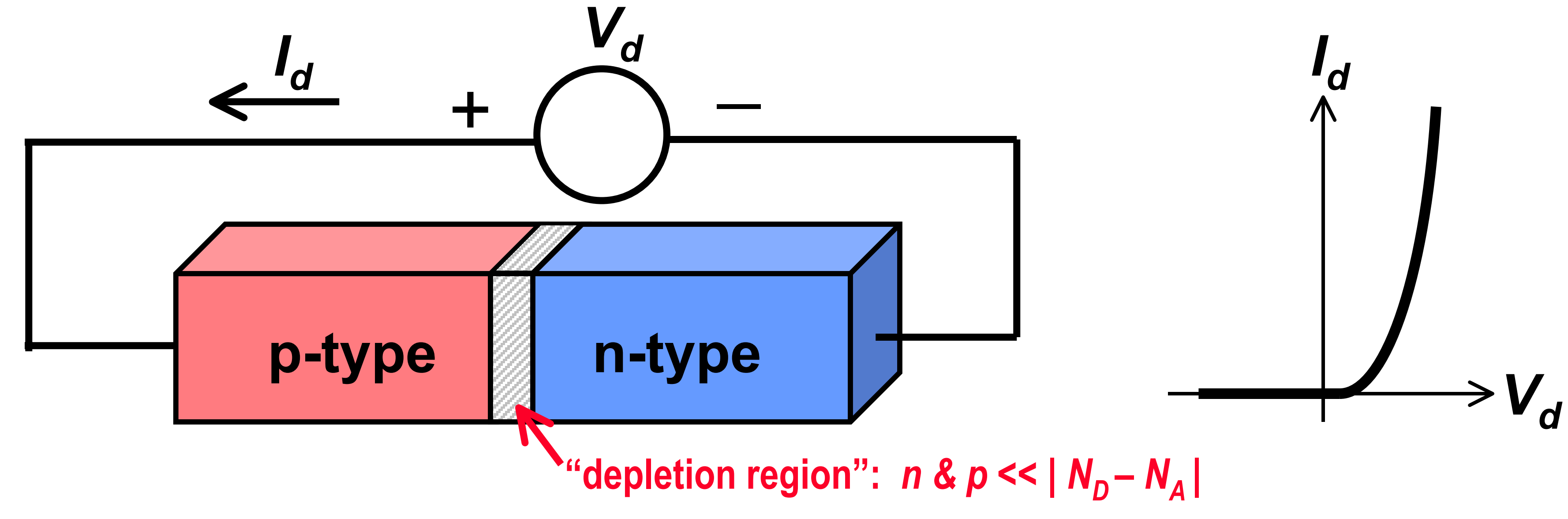
Notation	Interpretation
(***h k l***)	crystal plane
{ ***h k l*** }	equivalent planes
[***h k l***]	crystal direction
< ***h k l*** >	equivalent directions

h: inverse *x*-intercept
k: inverse *y*-intercept
l: inverse *z*-intercept

(Intercept values are in multiples of the lattice constant; *h*, *k* and *l* are reduced to 3 integers having the same ratio.)

Sample direction vectors and their corresponding Miller indices.

The pn-Junction Diode

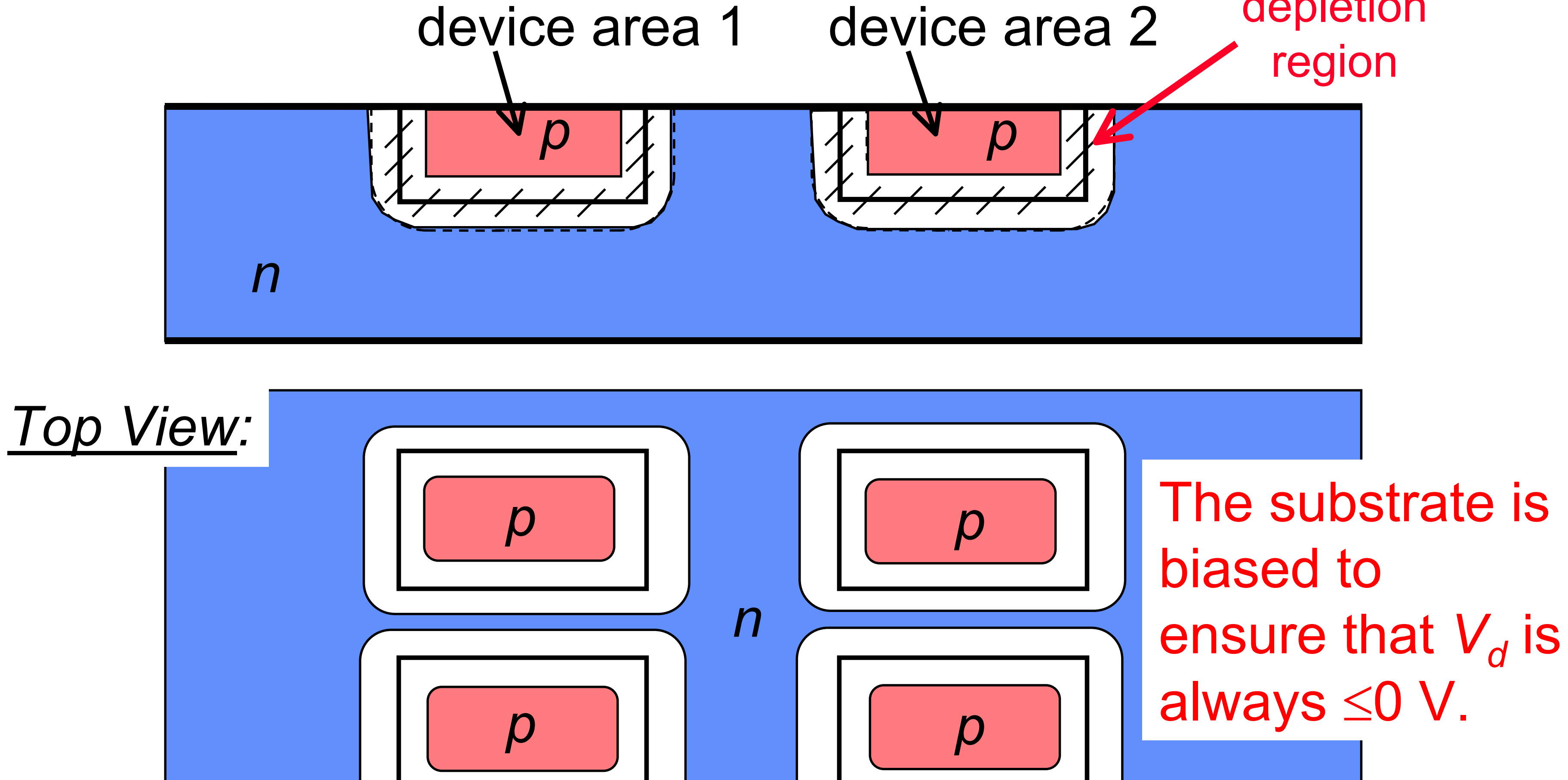


A *rectifying contact* is formed between a p-type region and an n-type region

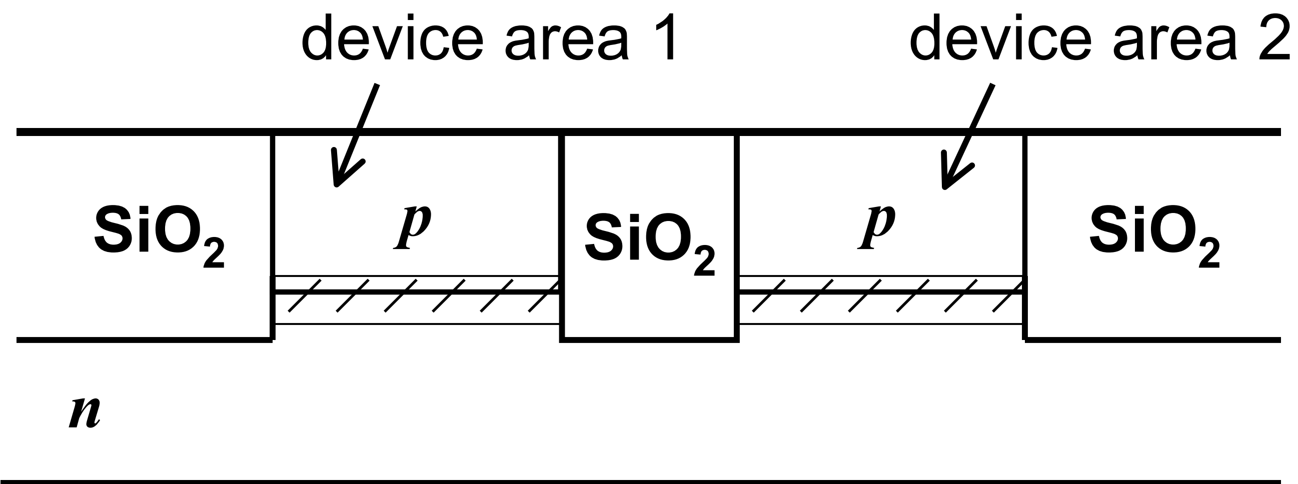
- Large current can flow in the direction from p to n
  - for V_d > ~0.7 Volts (Si diode)
- Negligible current flows in the direction from n to p
  - But for large negative V_d , the junction will eventually break down and conduct a large negative current

Device Isolation Methods

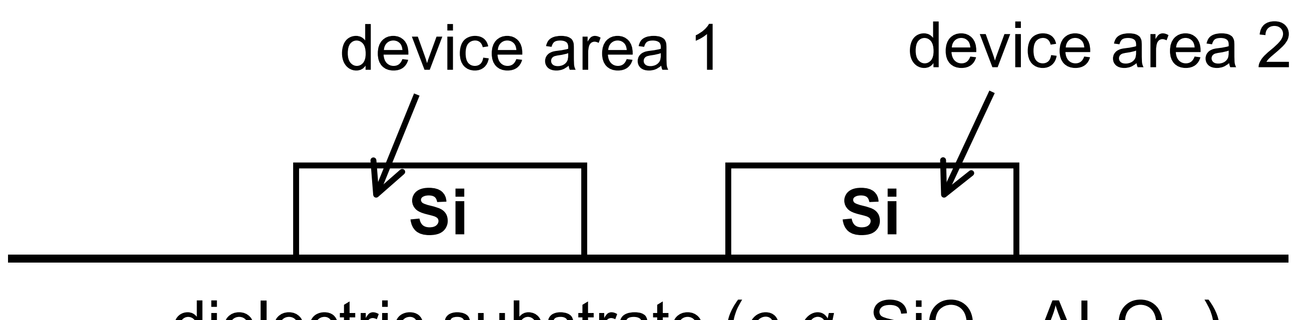
(1) pn-junction isolation:



(2) Oxide isolation:



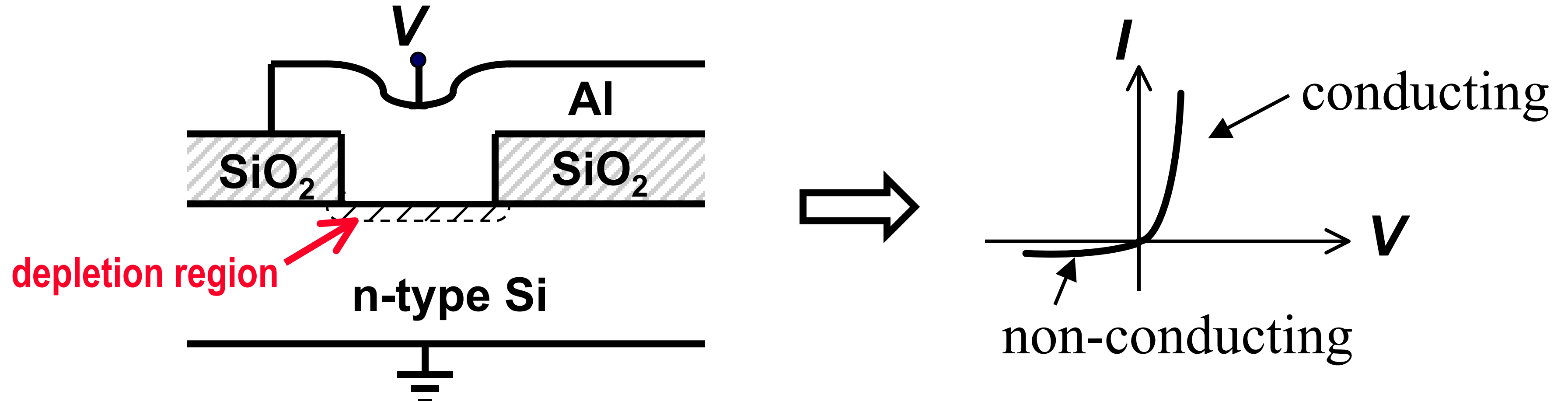
(3) Silicon-on-Insulator substrate:



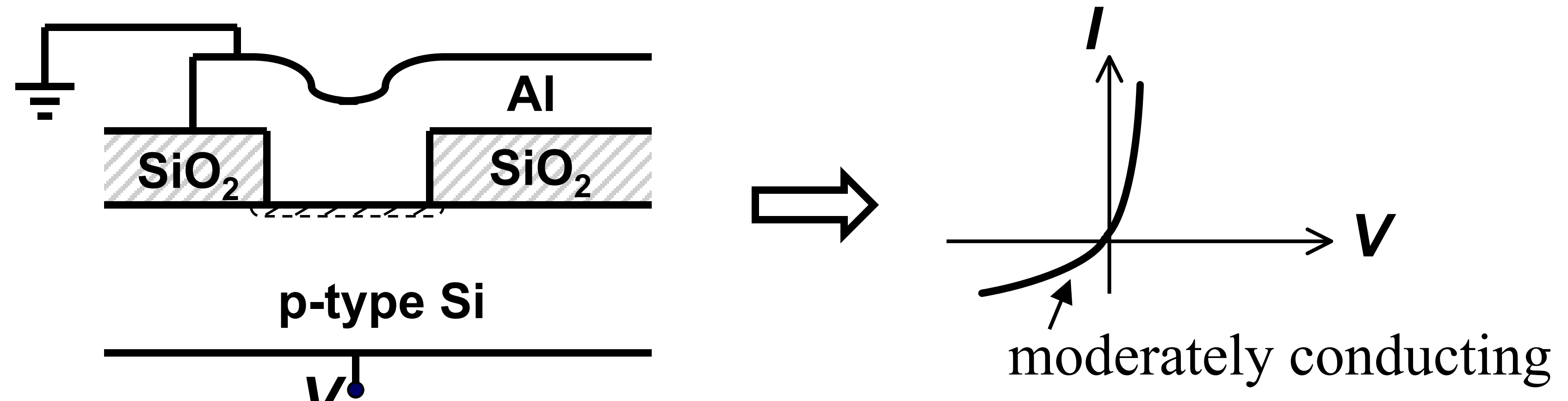
dielectric substrate (*e.g.* SiO_2, Al_2O_3)

Electrical Contacts to Si

(1) Schottky (rectifying) contacts:

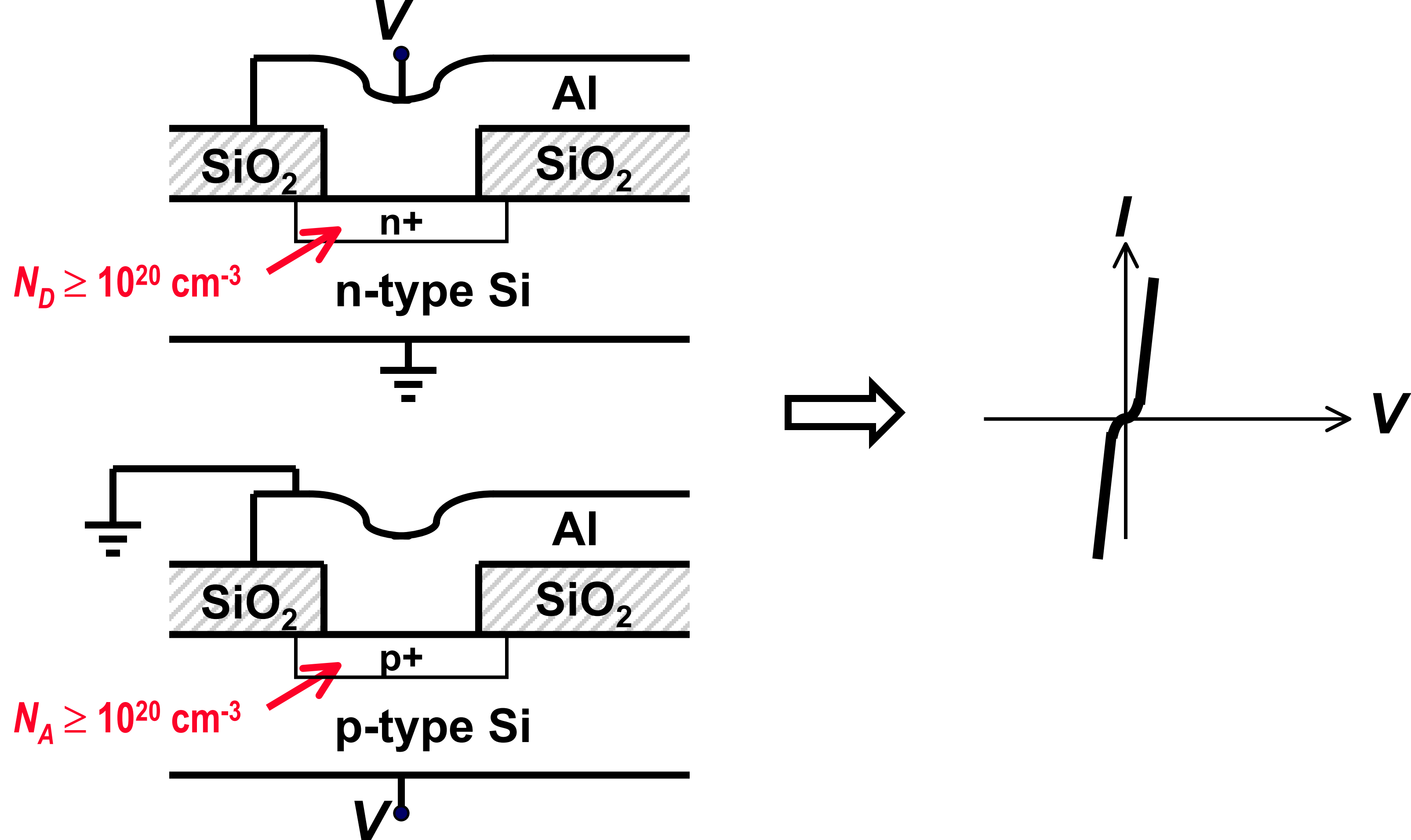


Majority carriers cannot move easily from the metal into the n-Si, due to a large potential barrier. For the same metal, this potential barrier is smaller for contacts to p-type Si.

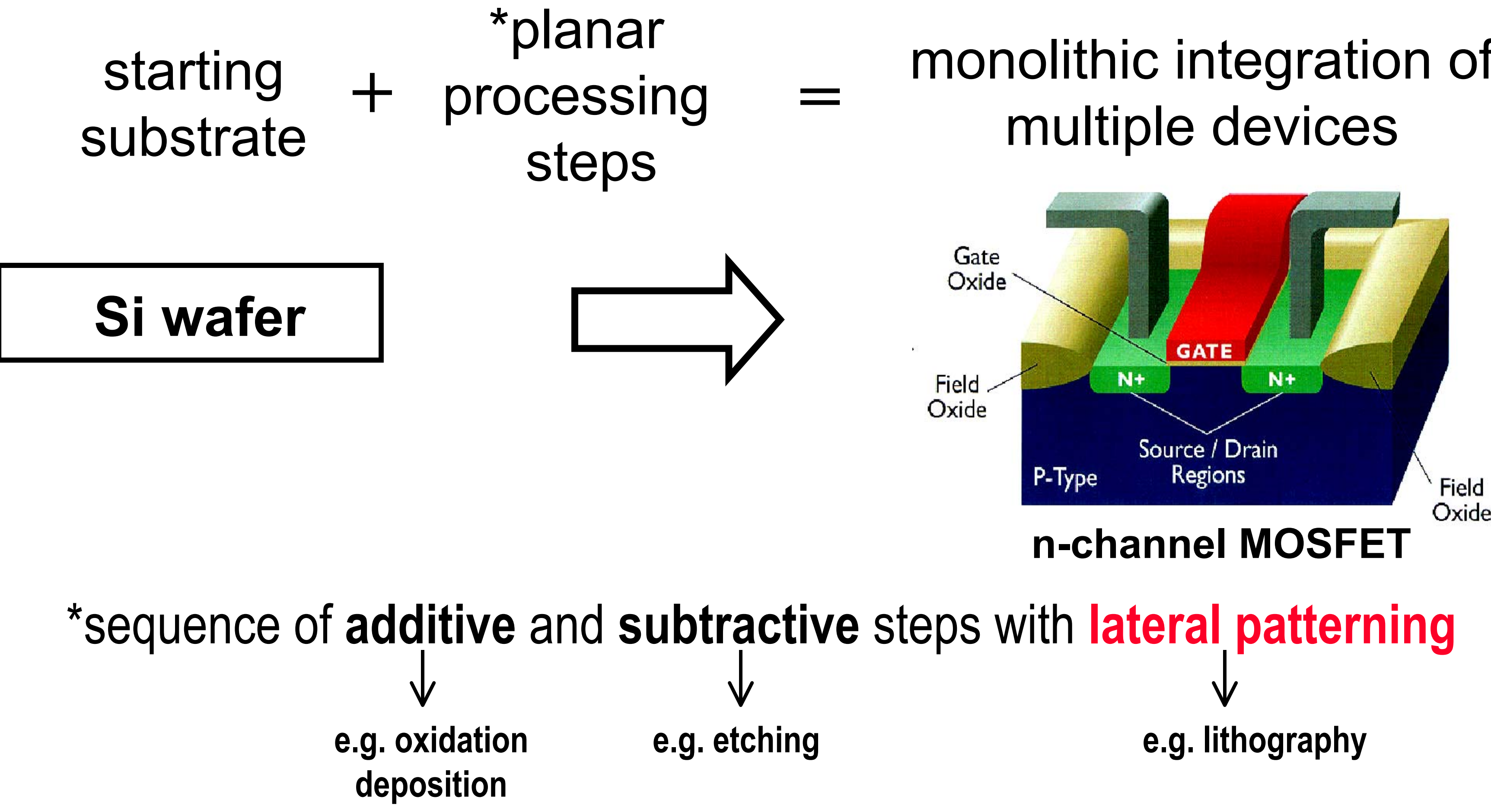


The depth of the depletion region (x_d) decreases with increasing dopant concentration. For very high doping, x_d is small enough (<10nm) to allow quantum tunneling of carriers.

(2) Tunneling "ohmic" contacts:

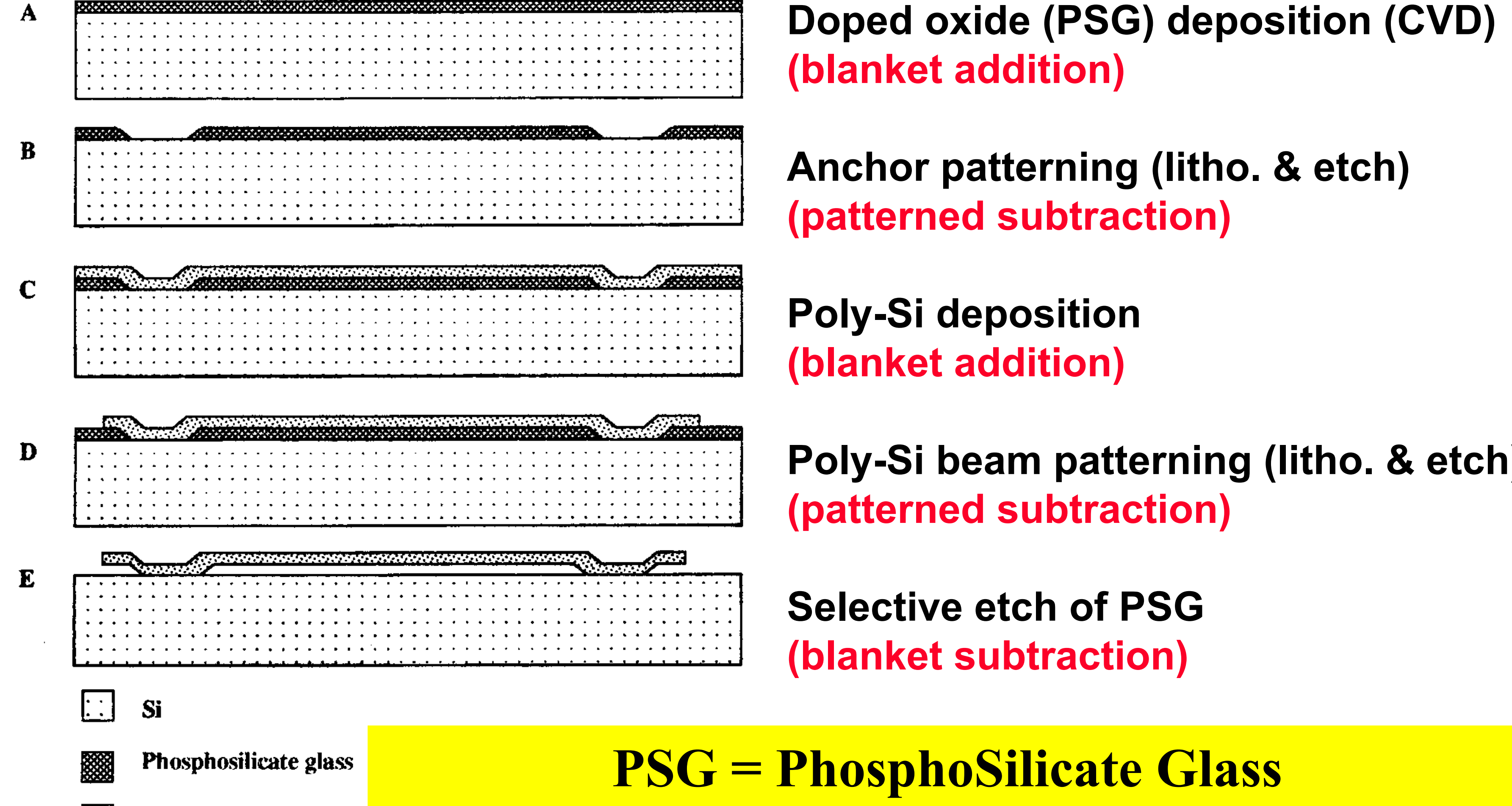


Planar Technology



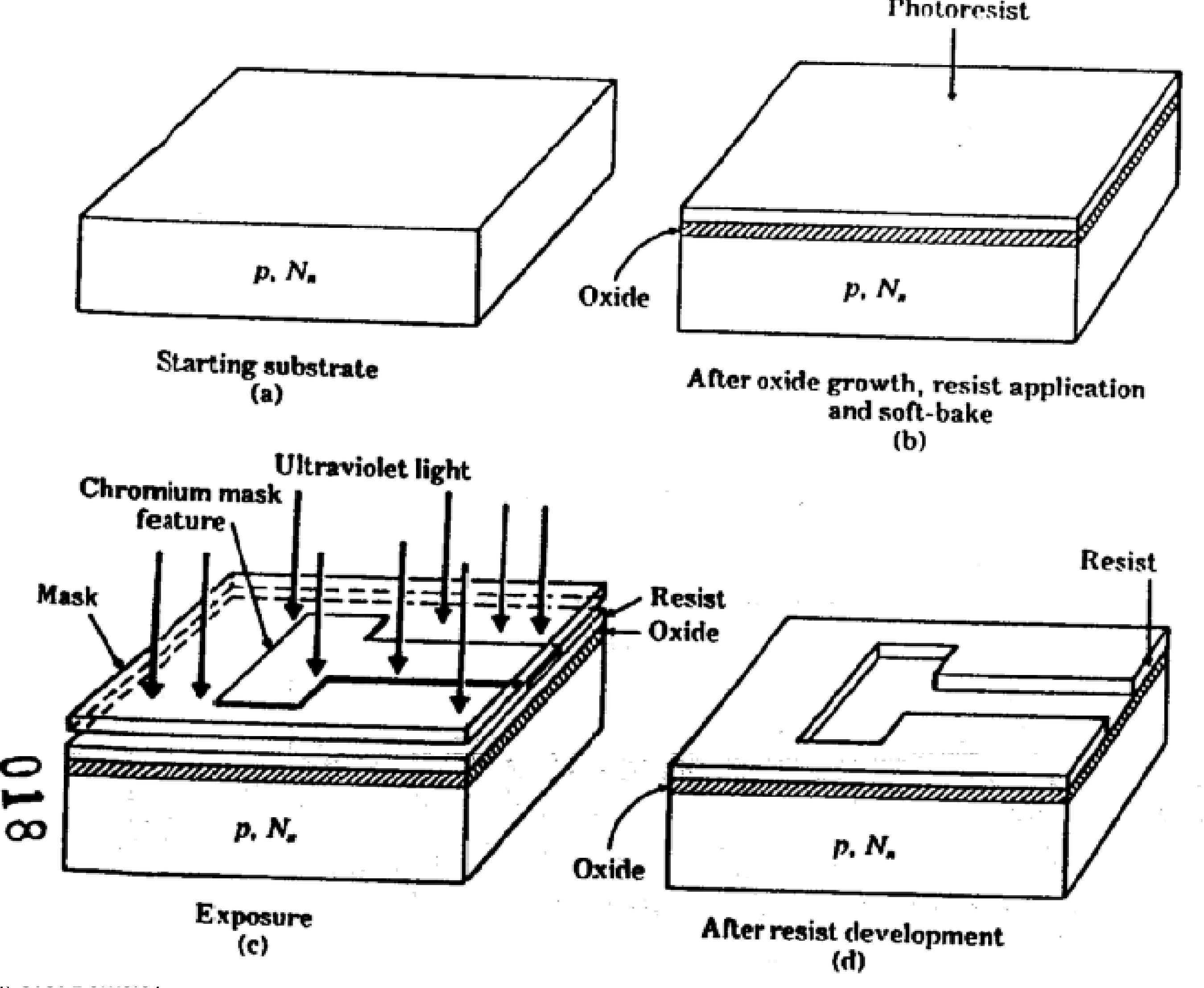
Process Flow Example #1

Suspended Beam Array



Process Flow Example #2

Al contact to n+ Si



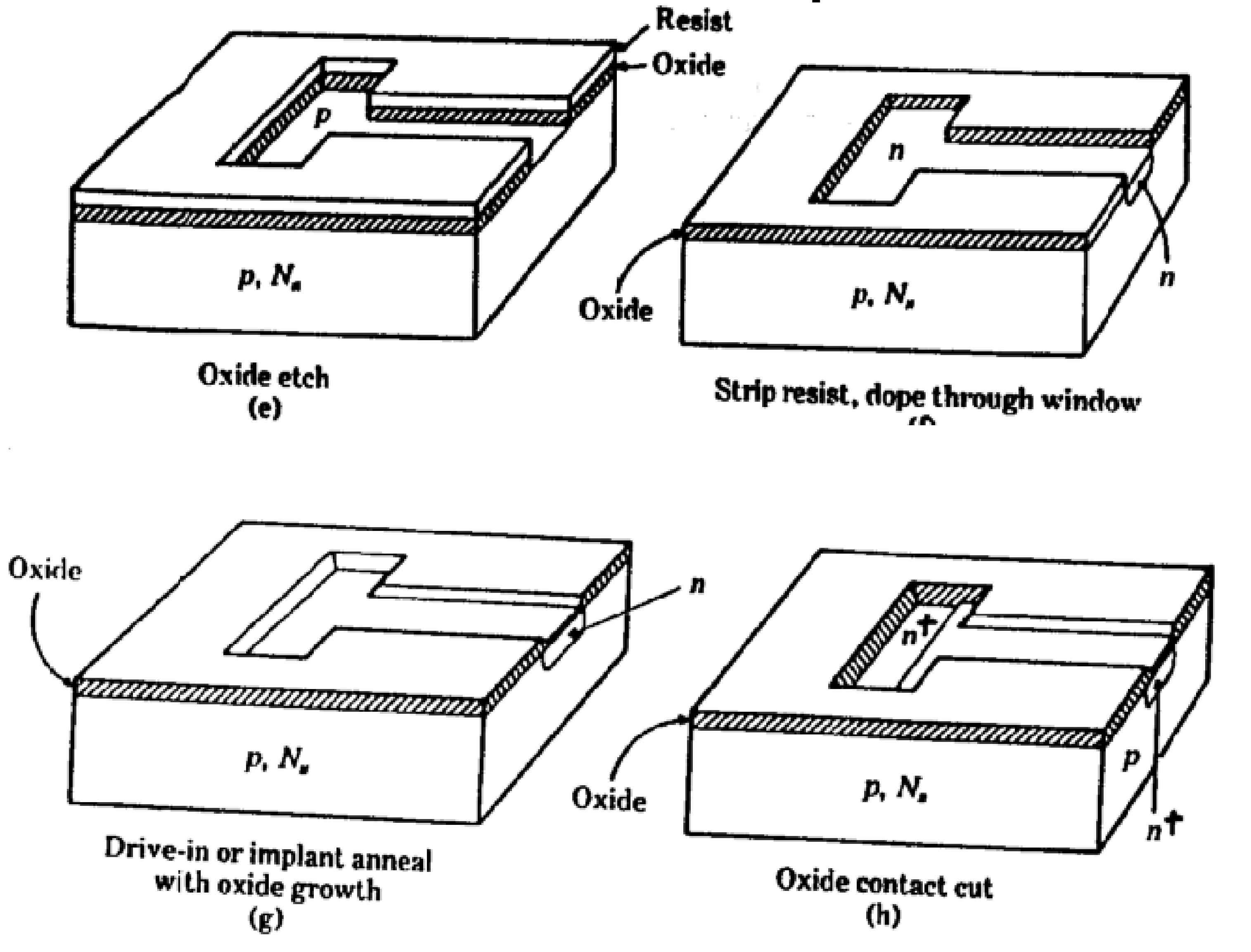
Starting substrate
(a)

After oxide growth, resist application and soft-bake
(b)

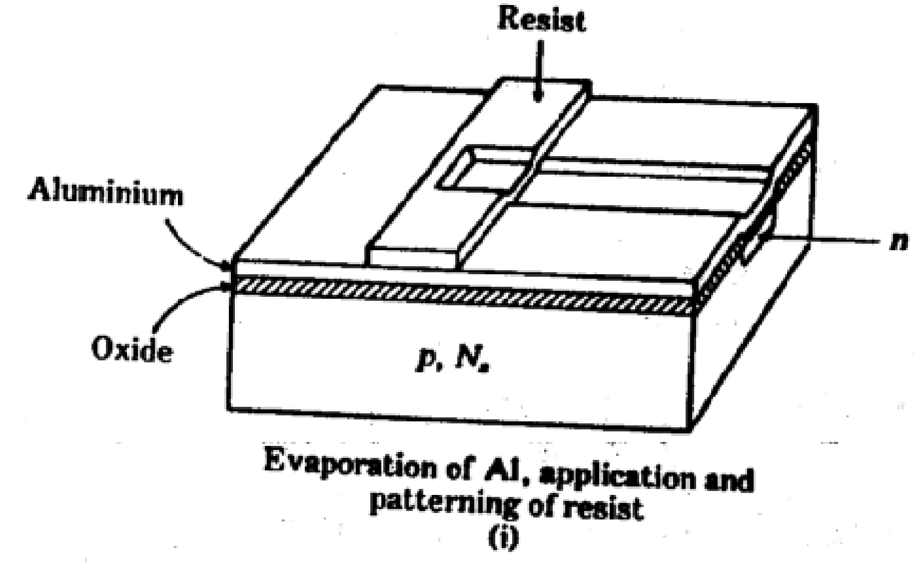
Exposure
(c)

After resist development
(d)

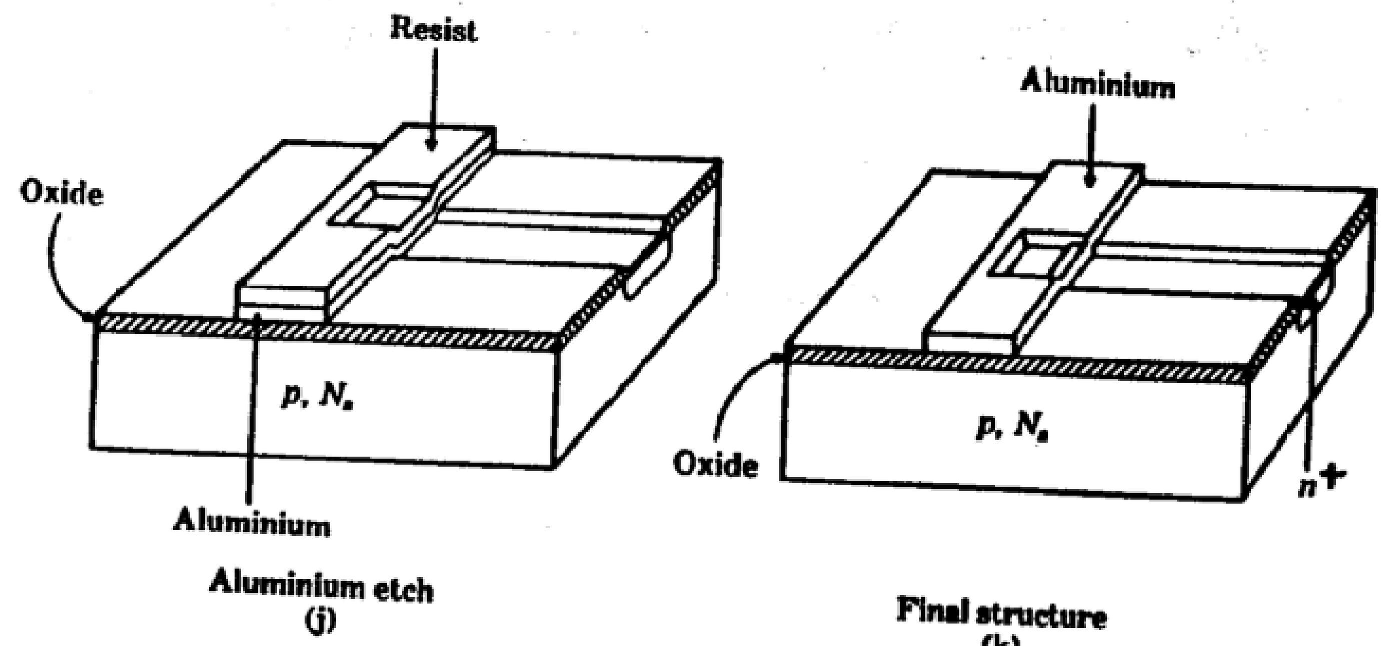
Process Flow Example #2 - cont



Process Flow Example #2 - cont



Evaporation of Al, application and patterning of resist
(i)

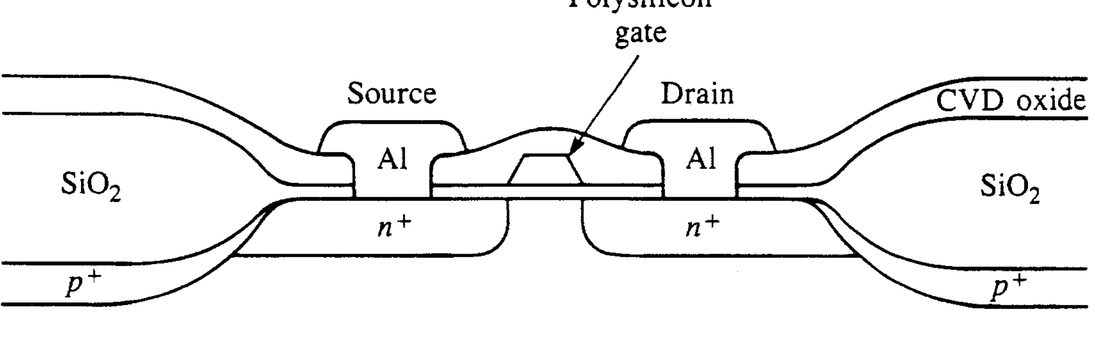


Aluminium etch
(j)

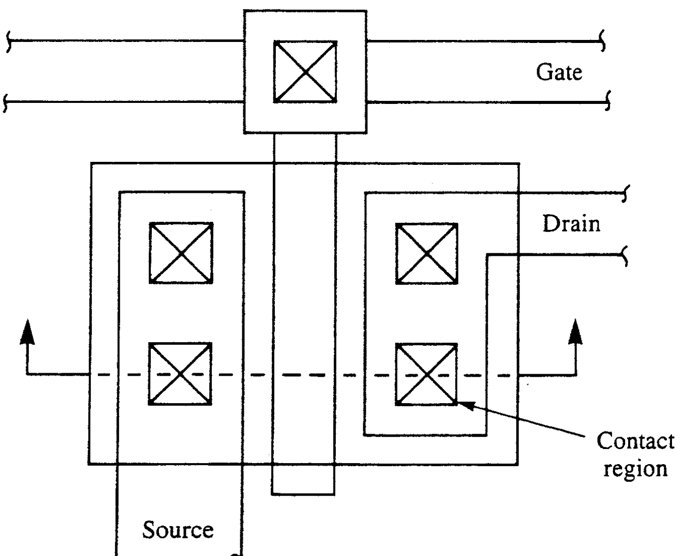
Final structure
(k)

N-channel MOSFET

Schematic Cross-Sectional View



Layout (Top View)



4 lithography steps are required:

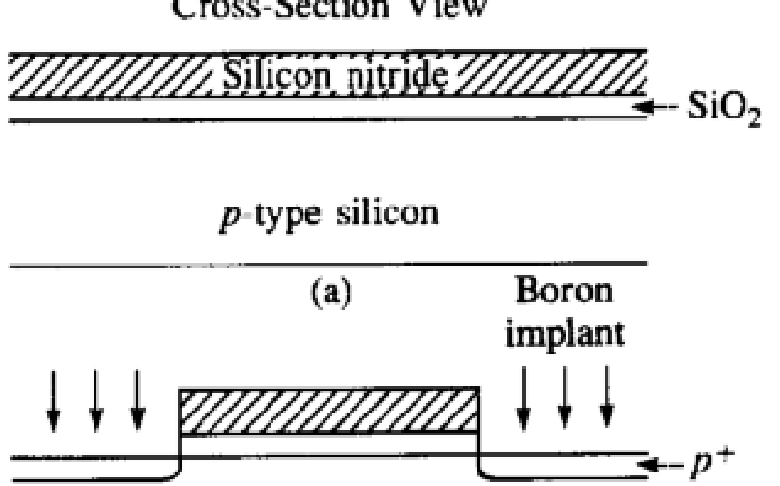
1. **active area**
2. **gate electrode**
3. **contacts**
4. **metal interconnects**

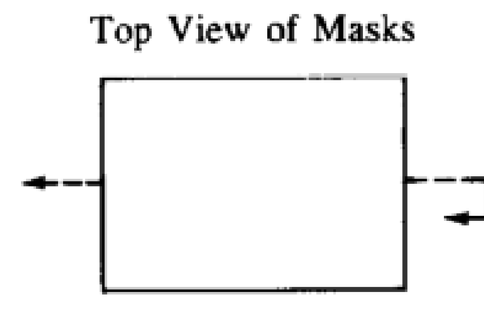
Process Flow Example #3

Simple nMOSFET Process Flow

Read Jaeger (textbook) Chap 1 for narrative description

1) **Thermal oxidation (~10 nm "pad oxide")**
2) **Silicon-nitride (Si_3N_4) deposition by CVD (~40nm)**
3) **Active-area definition (lithography & etch)**
4) **Boron ion implantation ("channel stop" implant)**





Process Flow Example #3 - cont

5) Thermal oxidation to grow oxide in “field regions”

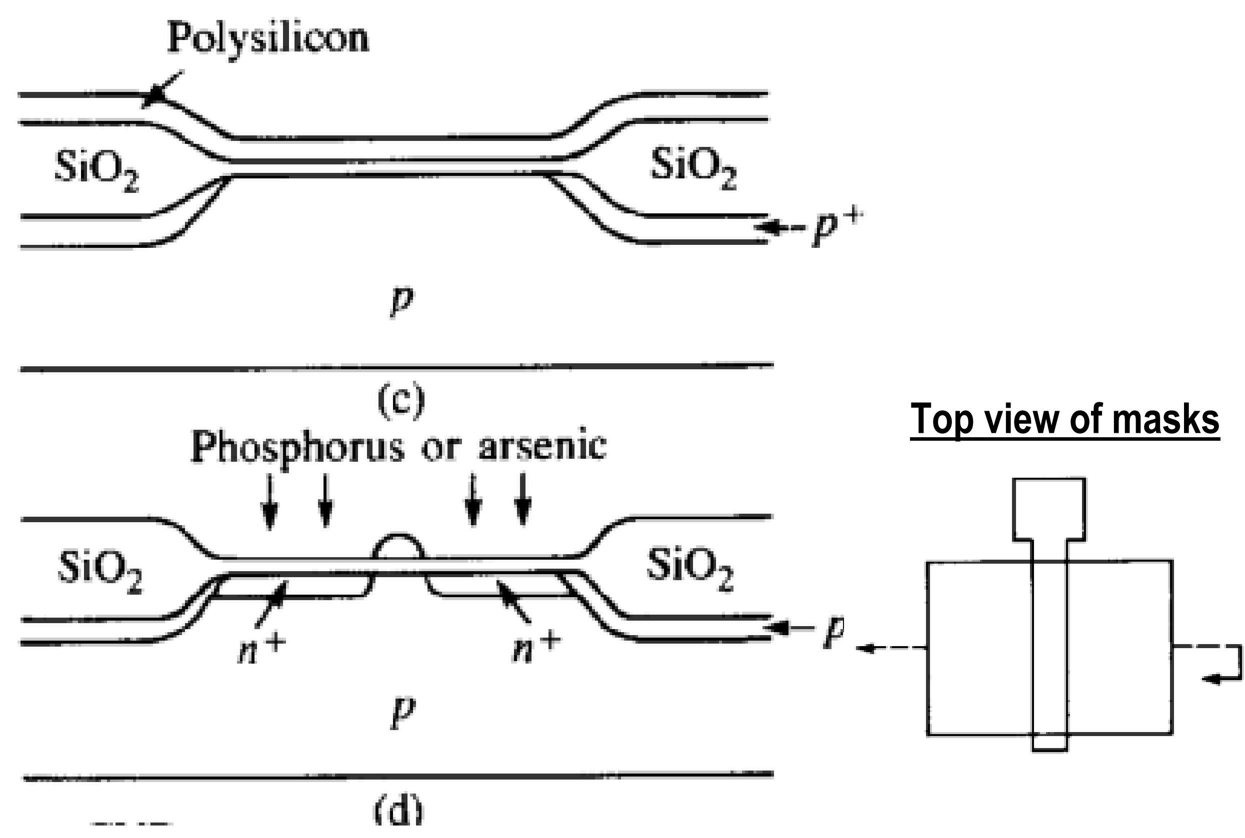
6) Si_3N_4 & pad oxide removal

7) Thermal oxidation (“gate oxide”)

8) Poly-Si deposition by CVD

9) Poly-Si gate-electrode patterning (litho. & etch)

10) P or As ion implantation to form n+ source and drain regions



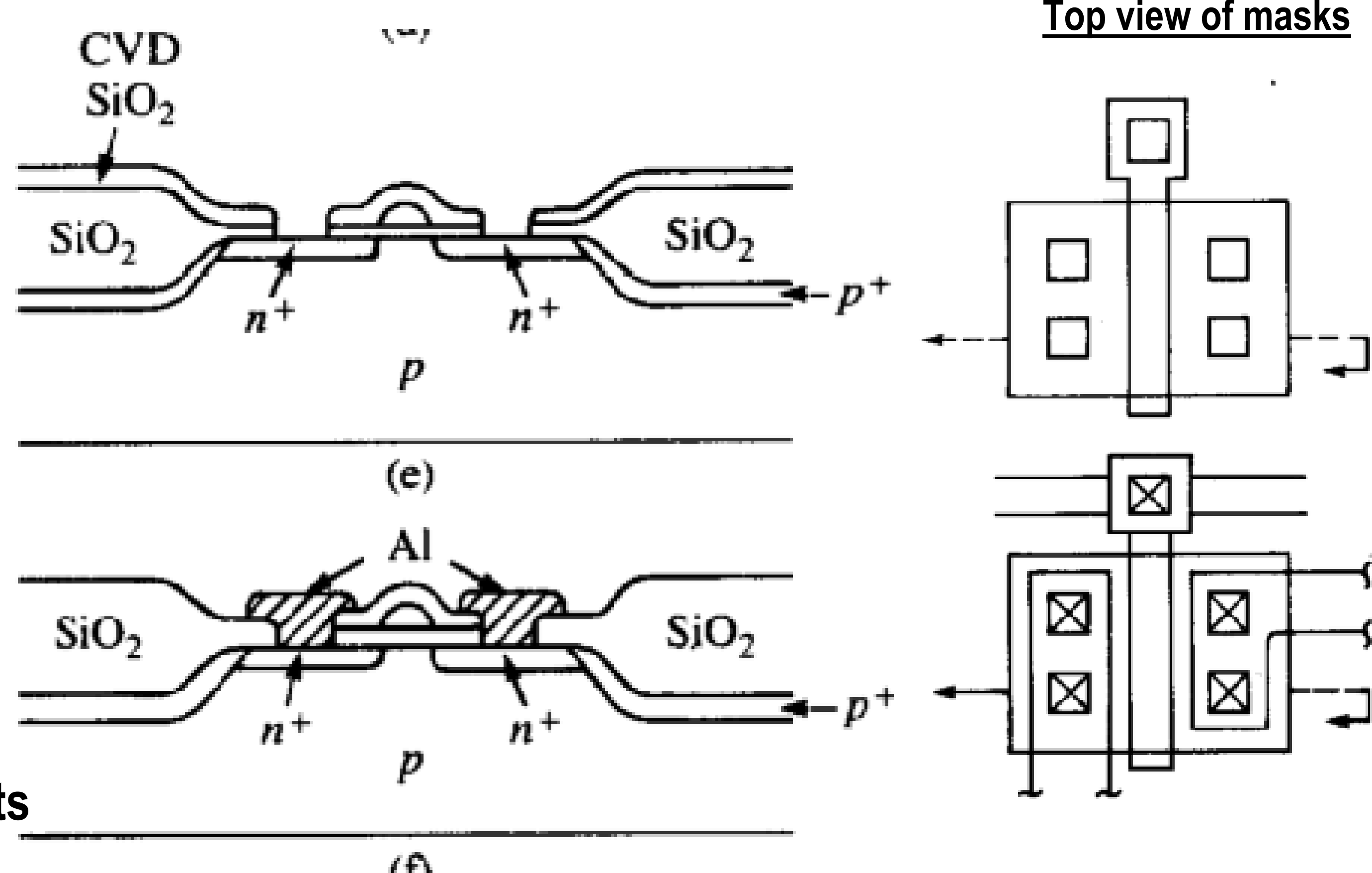
Process Flow Example #3 cont.

11) SiO_2 CVD

12) Contact definition (litho. & etch)

13) Al deposition by sputtering

14) Al patterning by litho. & etch to form interconnects



Process Flow Example #4

Plate
Staple
Hinge Plate

Hinged Structure

→ *out-of-plane movement*

3 Lithography steps:

1) **Hinge pattern**
2) **Staple anchor pattern**
3) **Staple pattern**