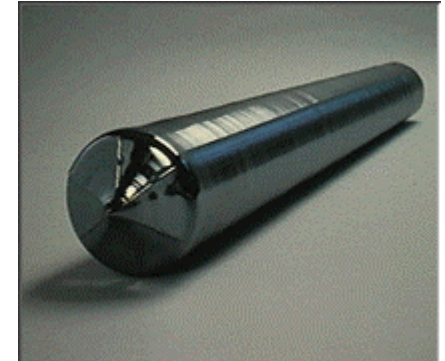
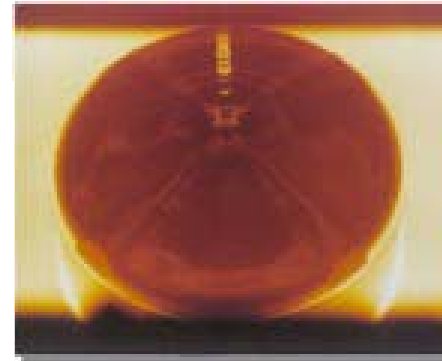
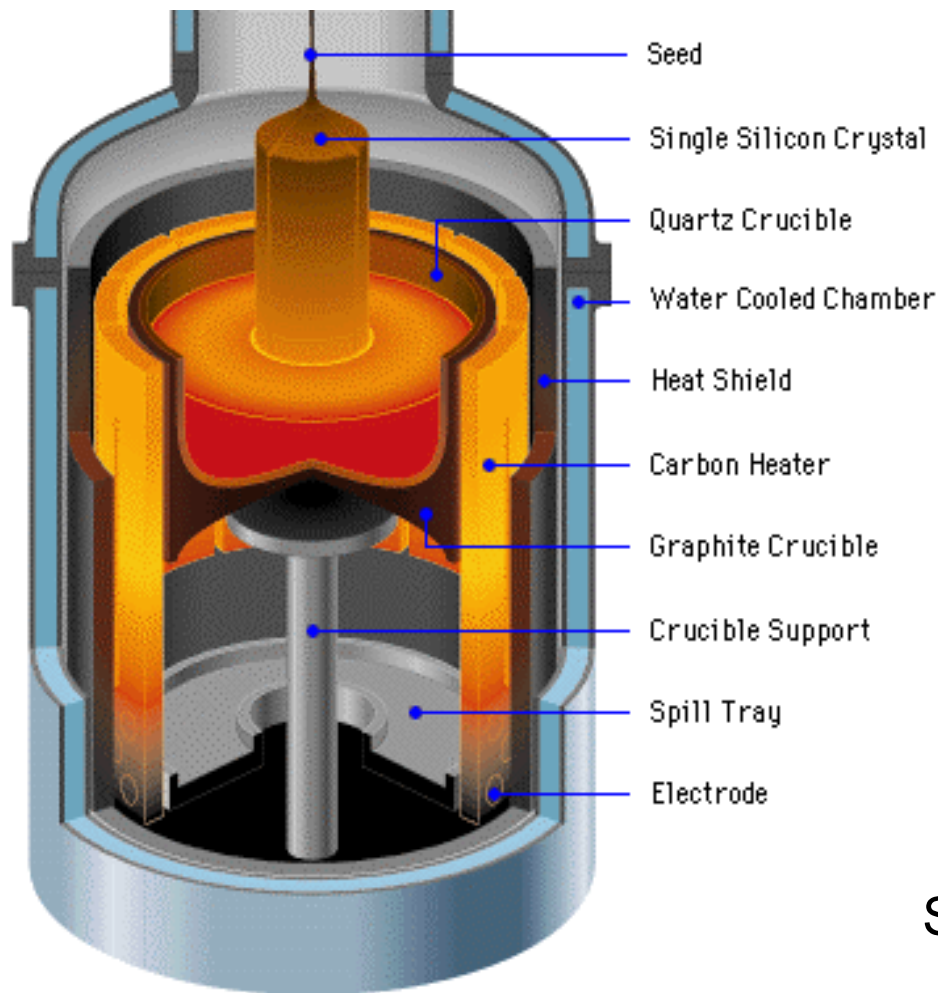


Czochralski Crystal Growth

Crystal Pulling

Crystal Ingots

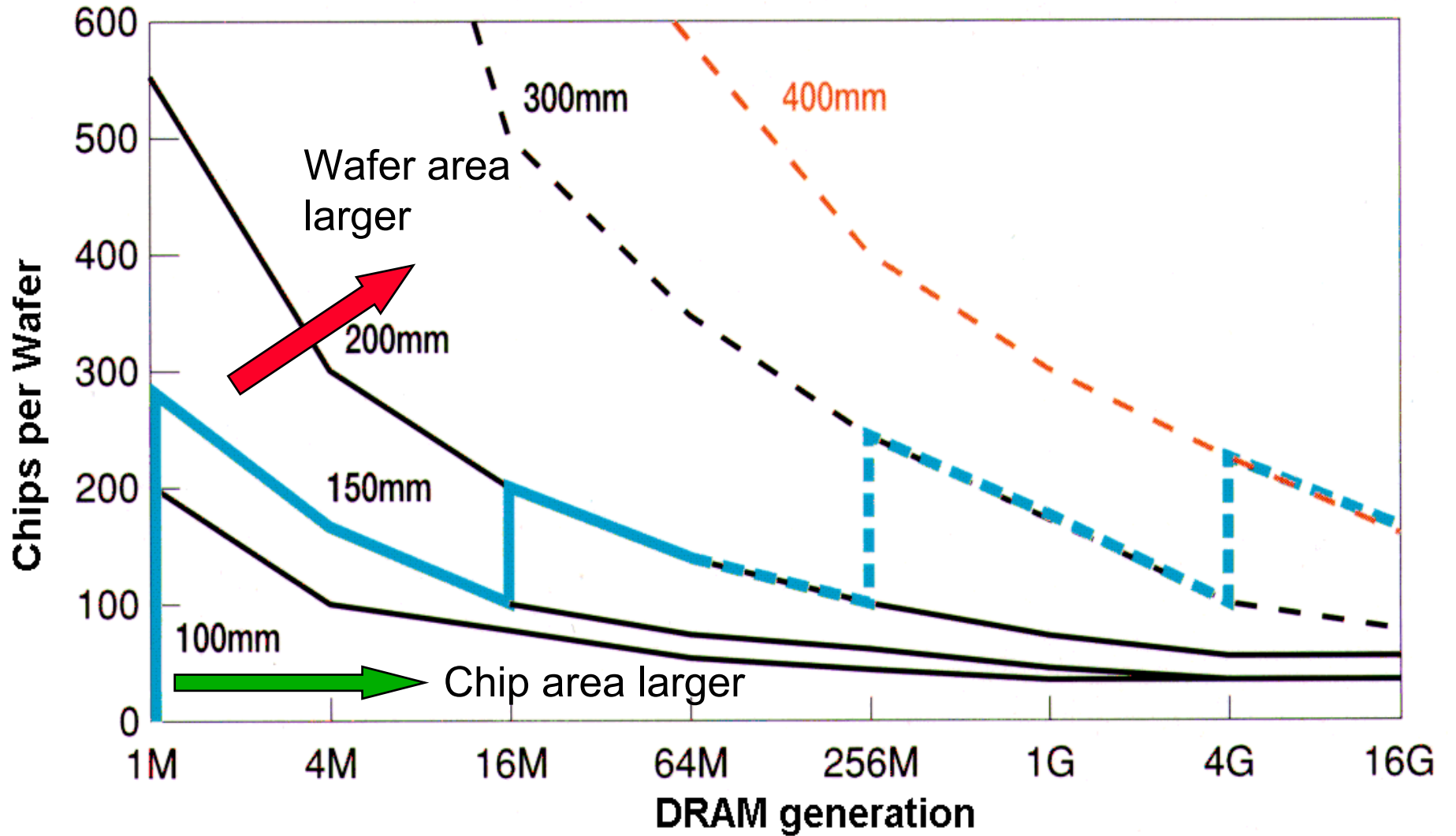


Shaping and Polishing



300 mm wafer

Advantage of larger diameter wafers



Large-Diameter Wafer Handling

La Vals Fab

Production Fab



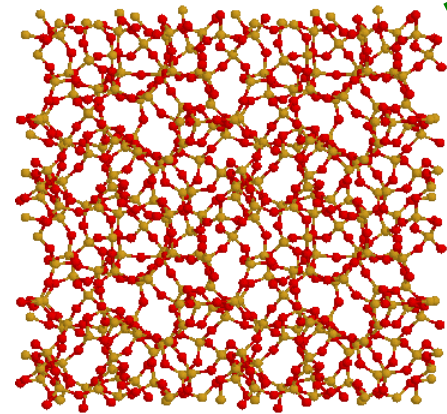
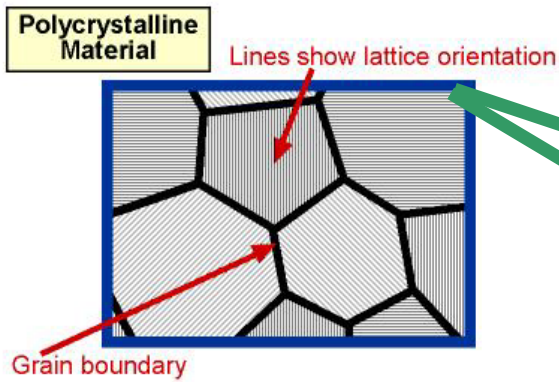
300mm wafer vs pizza



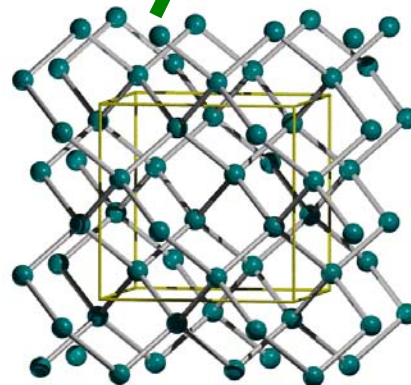
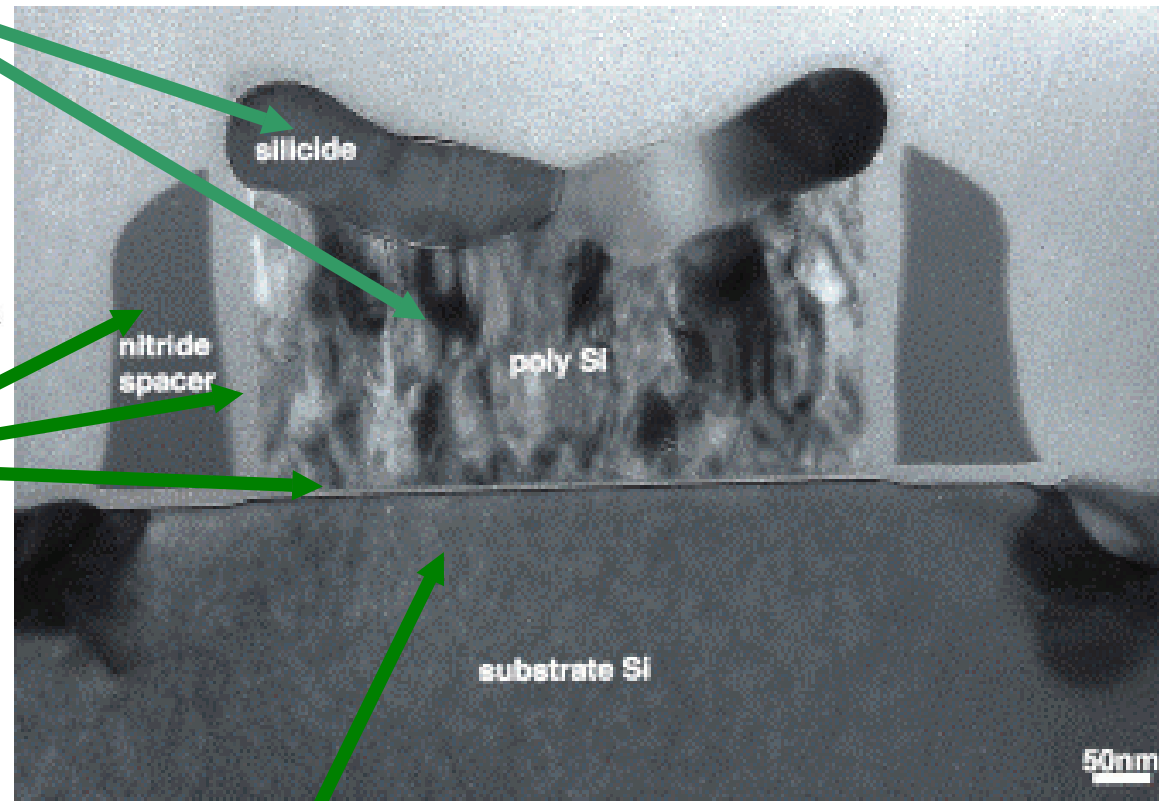
Overhead rail transport of wafer cassette

- Lateral uniformity of processing effects across the **WHOLE** wafer is key consideration for microfabrication design

Microstructure of Electronic Materials

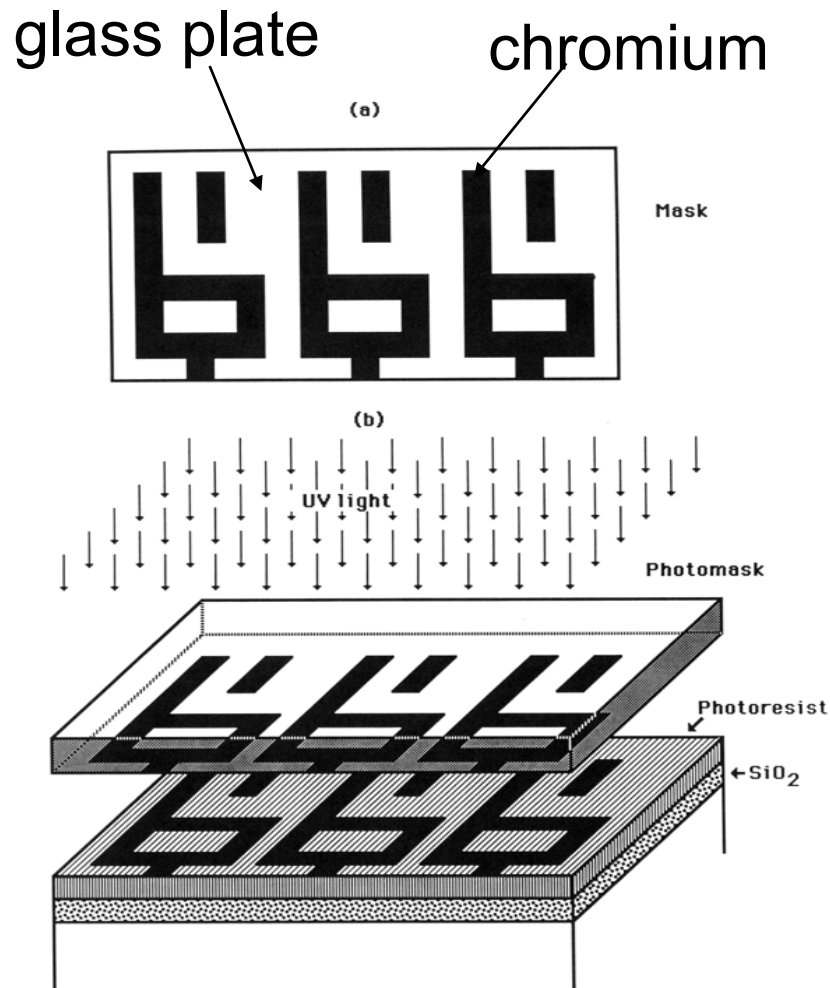


Amorphous materials



Single-Crystal Material

Photolithography



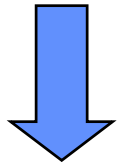
Positive Resist

Part exposed to light will be dissolved in development solution.

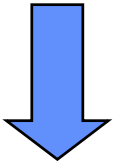
Processing Temperature
Ambient

Etching

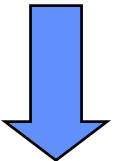
Pattern resist mask



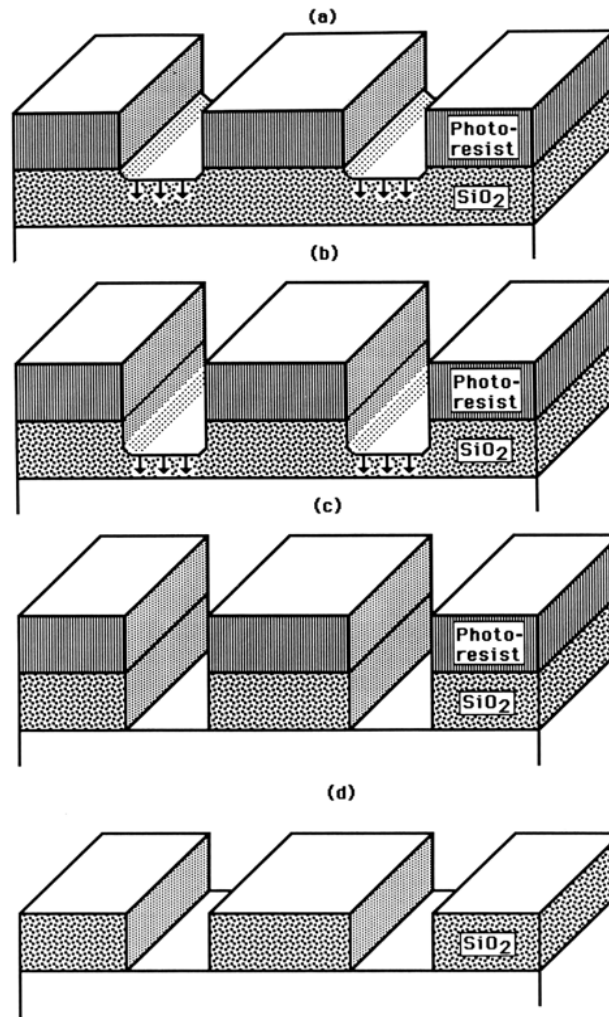
Etching thin film



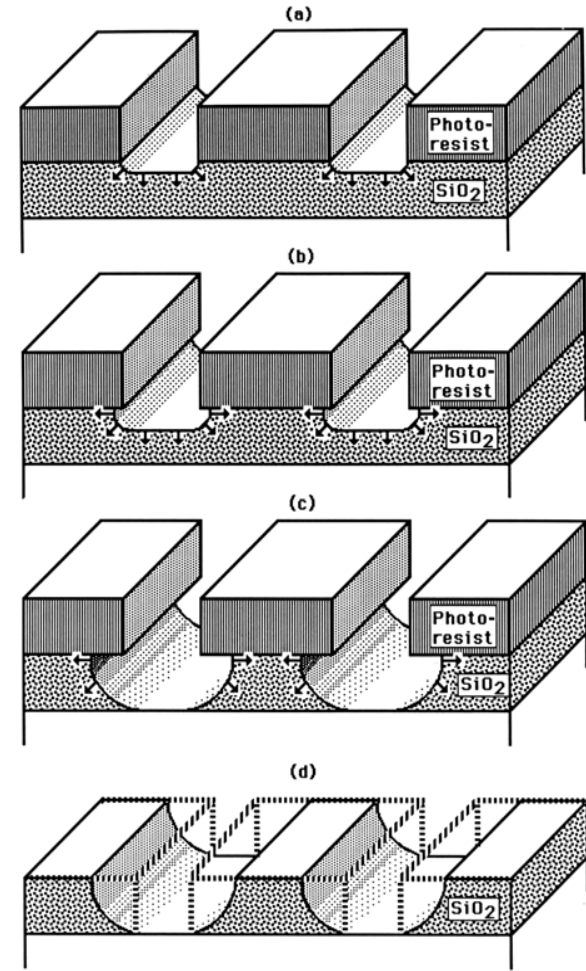
Etching completed



Remove resist mask



Anisotropic
(e.g. *Reactive Ion Etching*)

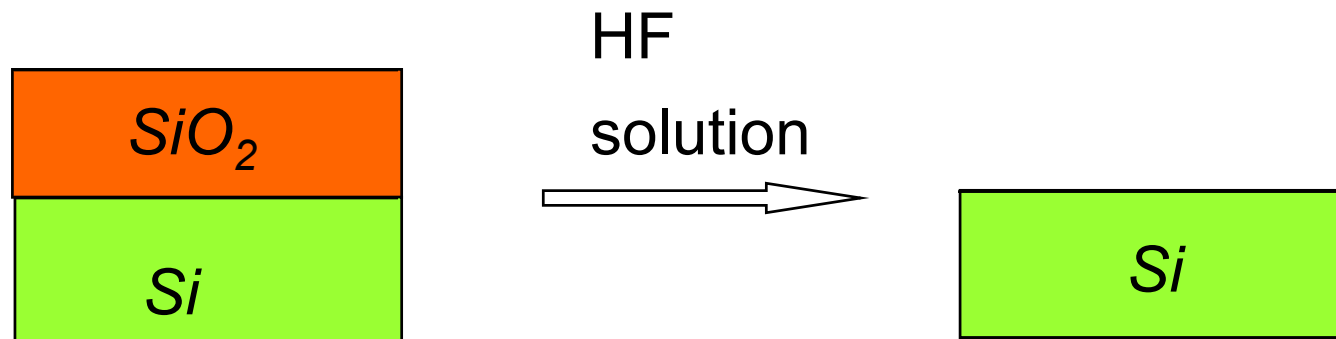


Isotropic
(e.g. *Wet Etching*)

Processing Temperature
Ambient

Etching Selectivity

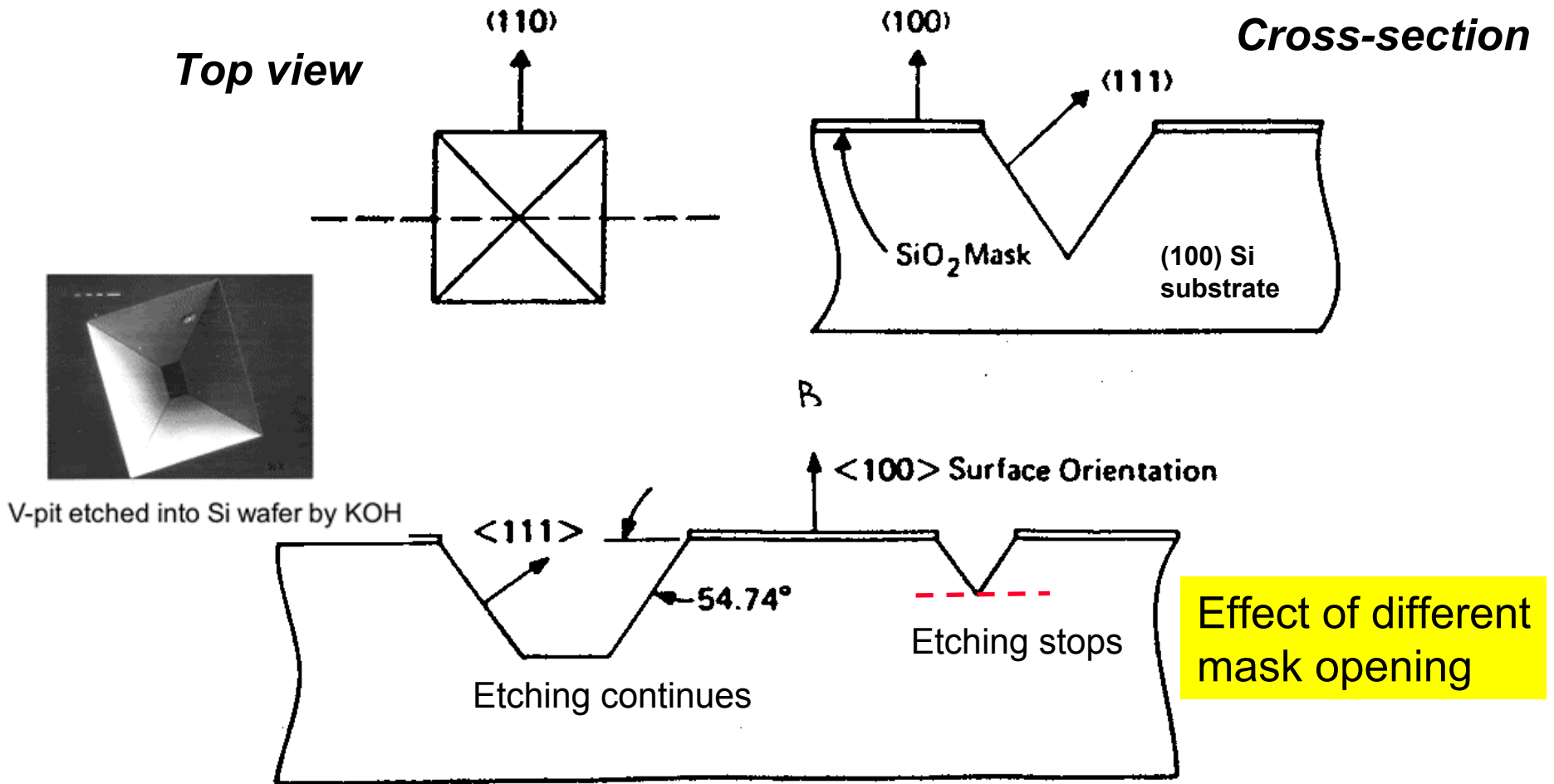
Example: HF solution etches SiO_2 but not Si



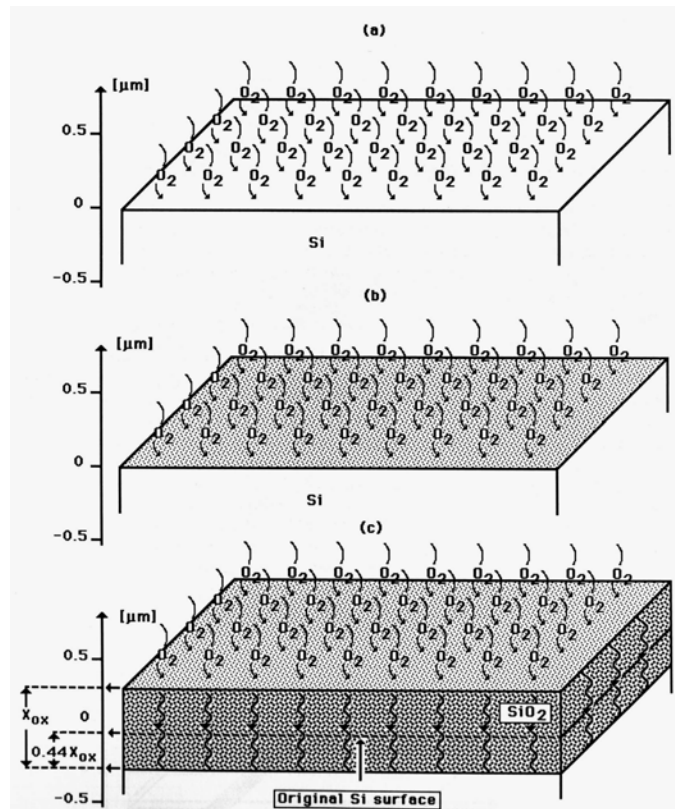
* A high etching selectivity is usually desired

“Anisotropic “ Wet Etching of Si Crystals

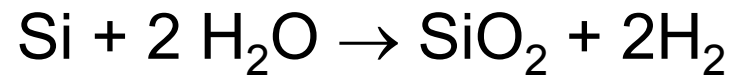
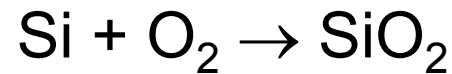
Etchants : KOH or EDP (Ethylene-Diamine_Pyrocatechol)



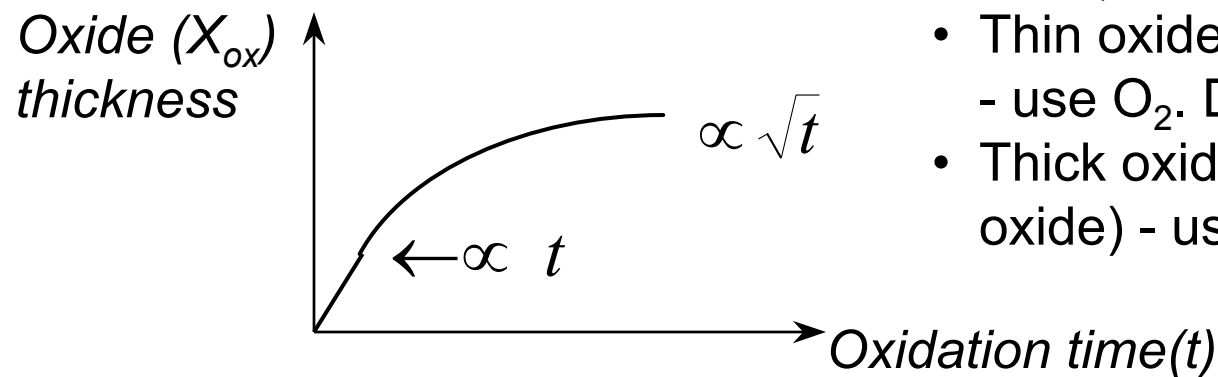
Thermal Oxidation



Processing Temperature
900-1100 °C

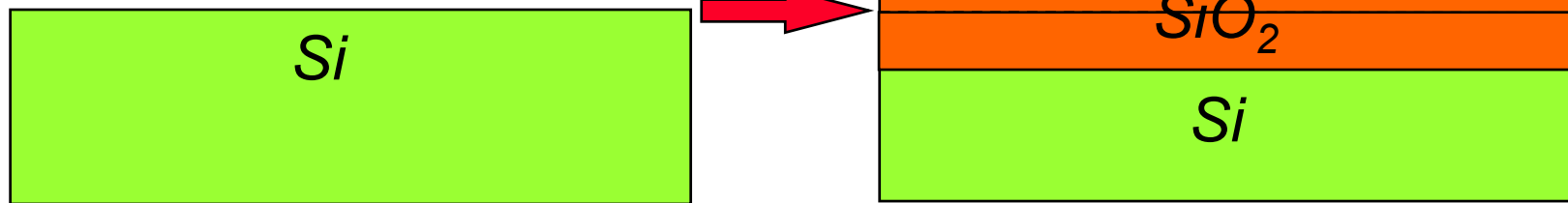


- O₂ (or H₂O) diffuses through SiO₂ and reacts with Si at the interface to form more SiO₂.
- 1 μm of SiO₂ formed consumes 0.44 μm of Si substrate.
- Thin oxide growth (e.g. gate oxide) - use O₂. Dry oxidation
- Thick oxide growth (e.g. field oxide) - use H₂O. Wet oxidation



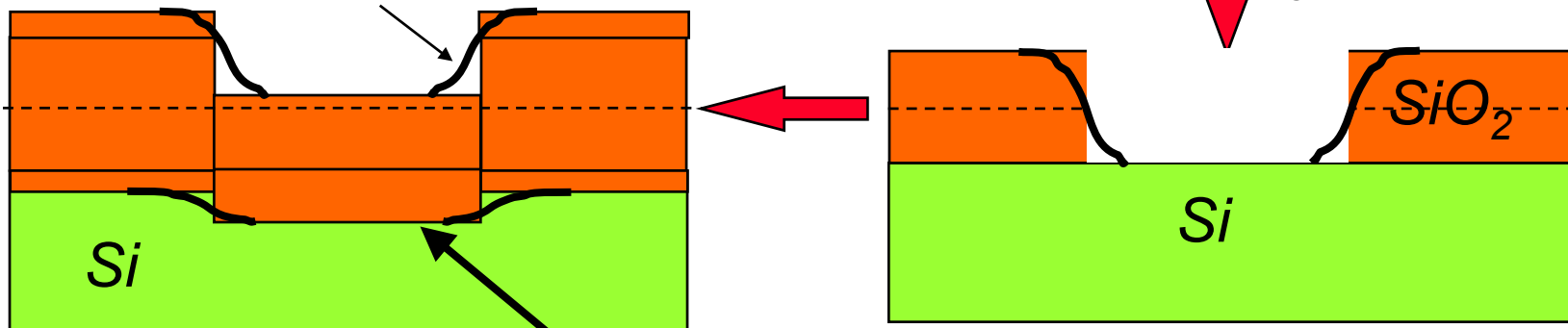
Uneven surface topography with window oxidation

1st oxidation



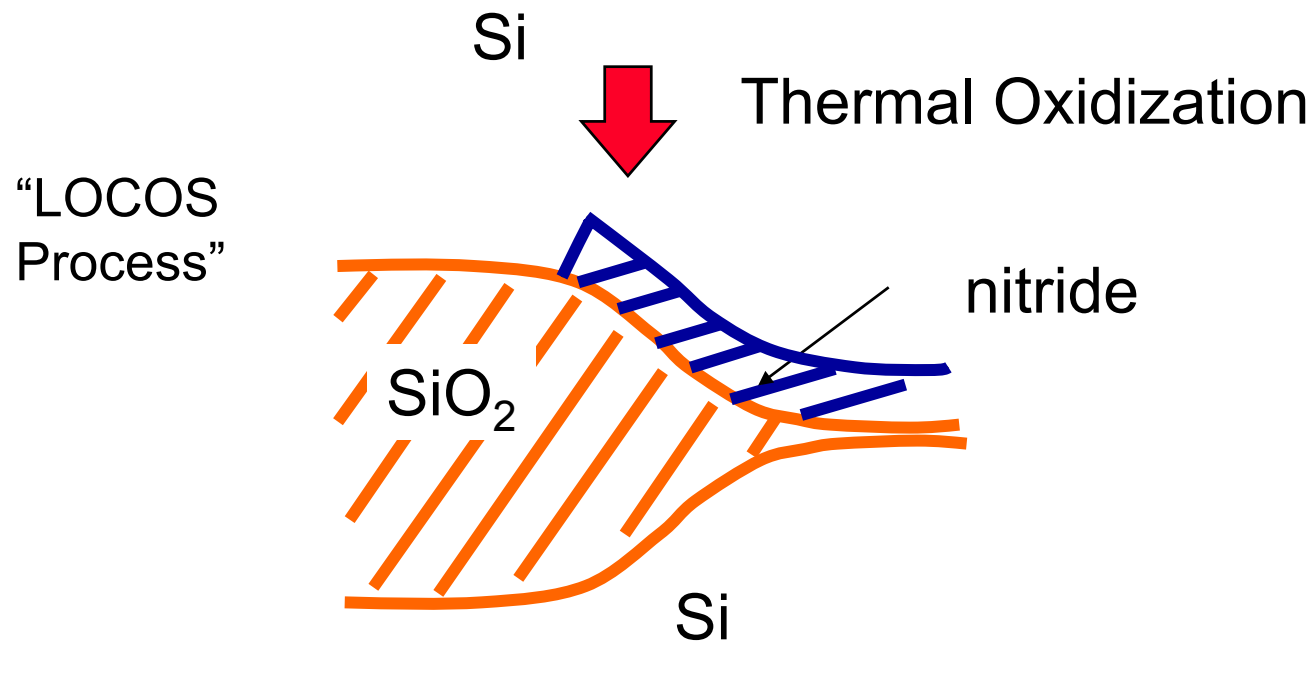
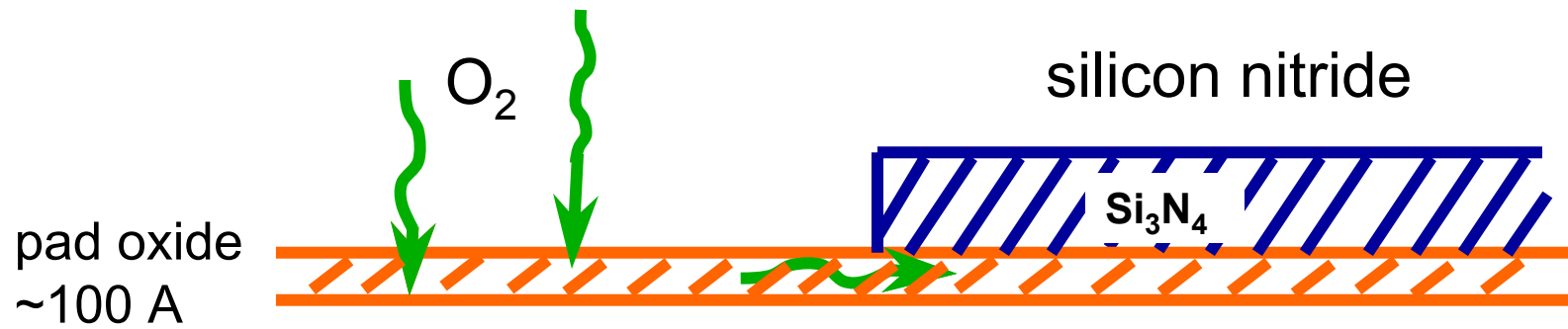
Realistic topography
with 2-dimensional effect

2nd oxidation



Note uneven Si surface
after window oxidation

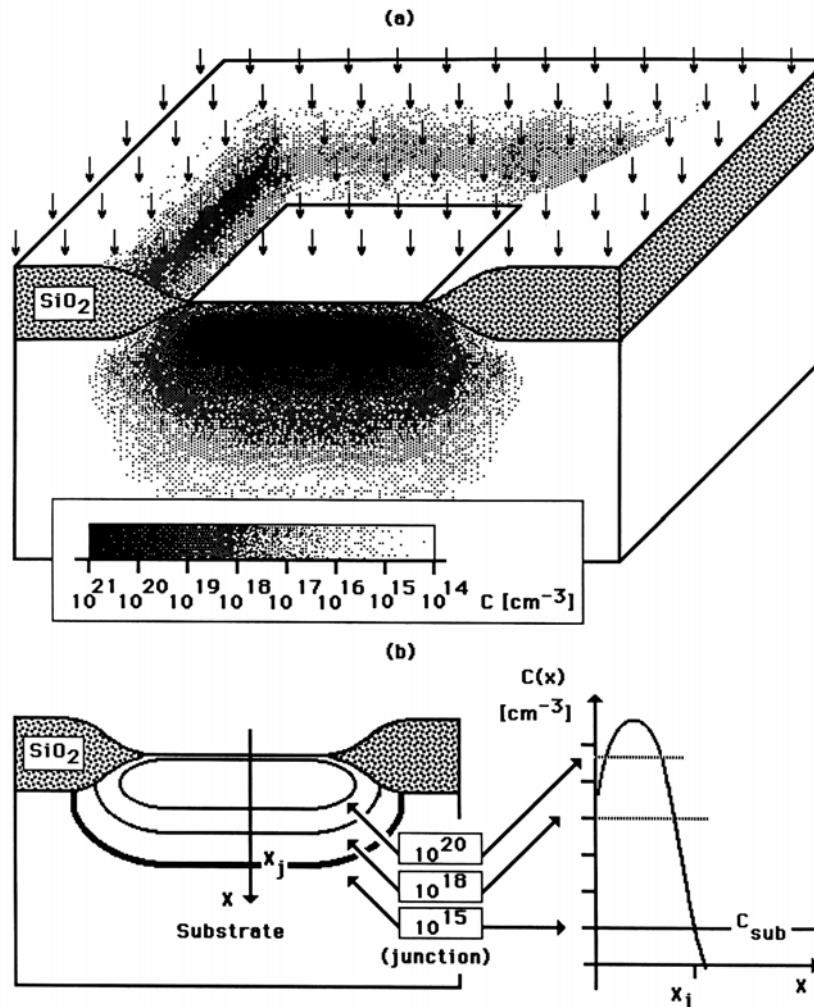
Local Oxidation



Ion Implantation

typically used to introduce dopants into semiconductors

Ion Energy
~1 keV to
200 keV



Processing Temperature

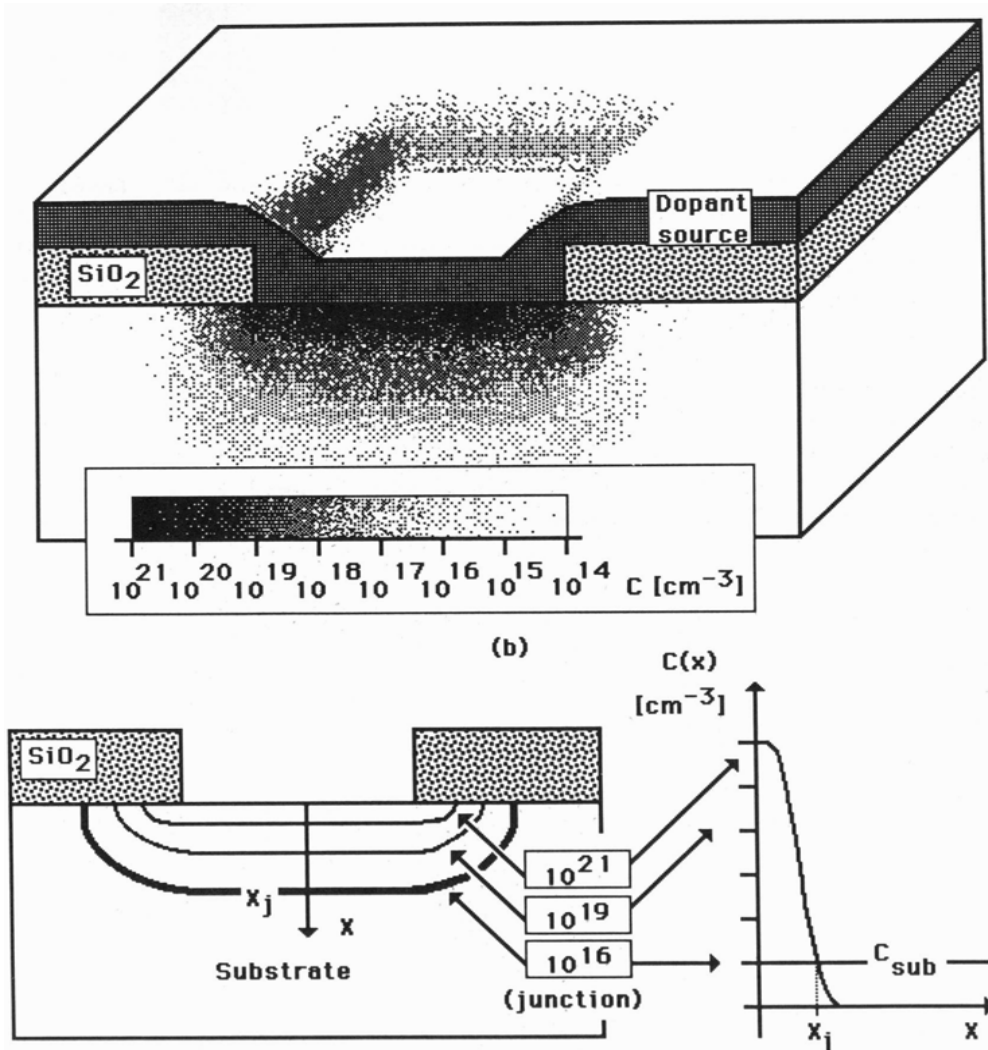
Room temp during
implantation.

After implantation,
a 900°C-1000°C
anneal step is needed to:

- 1) activate dopants
- 2) restore Si crystallinity

Diffusion

- To introduce dopants into semiconductors [**Predeposition**]
- To spread out the dopant profile [**Drive-in**]



$$D = D_0 \cdot e^{-Q/kT}$$

$D =$ Diffusion Constant

$Q =$ Activation Energy

$T =$ Temp in K ($D \uparrow$ as $T \uparrow$)

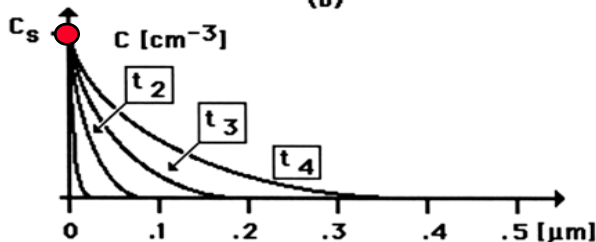
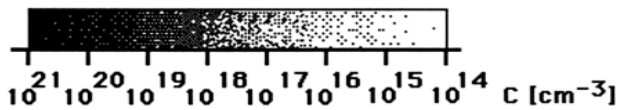
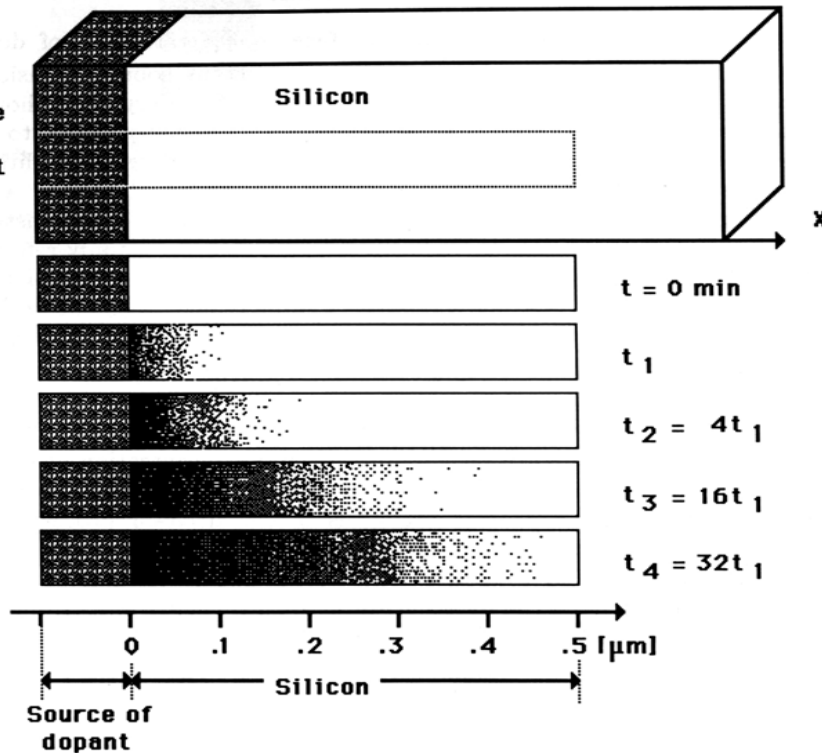
Processing Temperature
950-1200 °C

Predeposition

- Si surface concentration maintained at constant C_s (solid-solubility) during predep.

- Dose of dopant incorporation

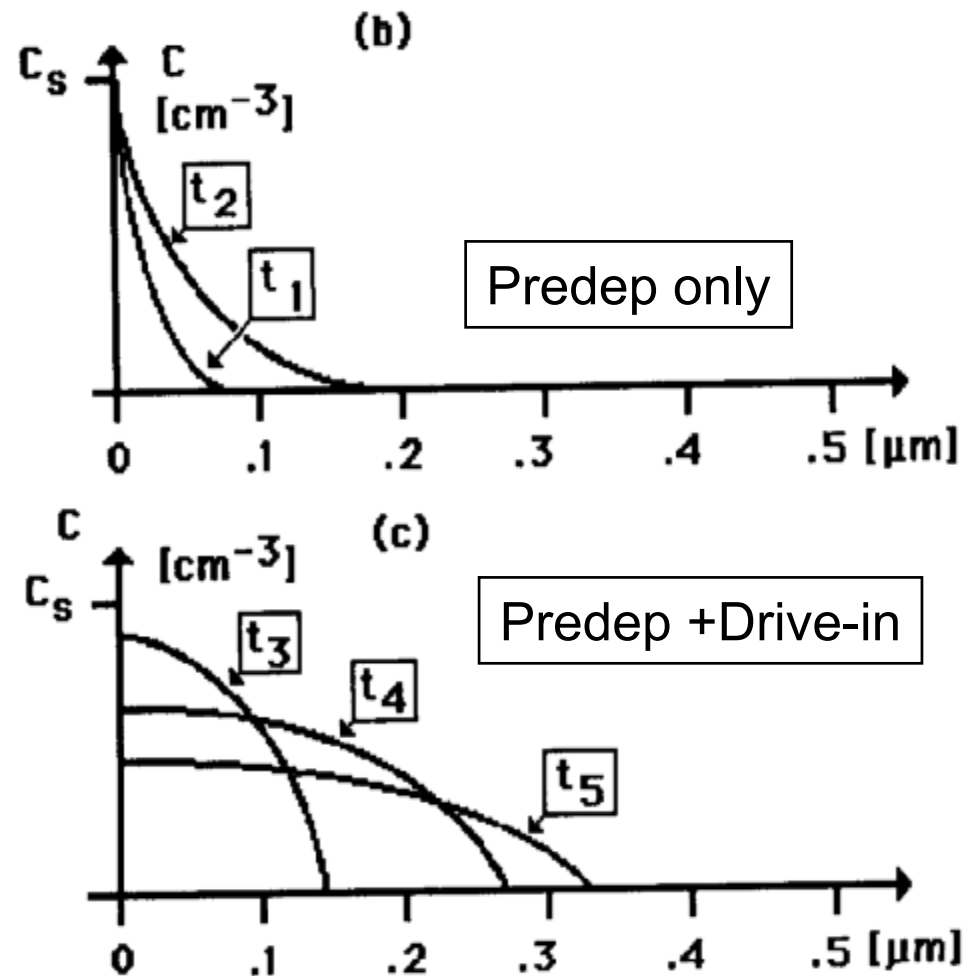
$$= \frac{C_s \cdot 2\sqrt{Dt}}{\sqrt{\pi}}$$



Predeposition and Drive-in

- Half-gaussian depth profile after long drive-in.
- Dopant dose **conserved** during drive-in.
- Diffusion distance

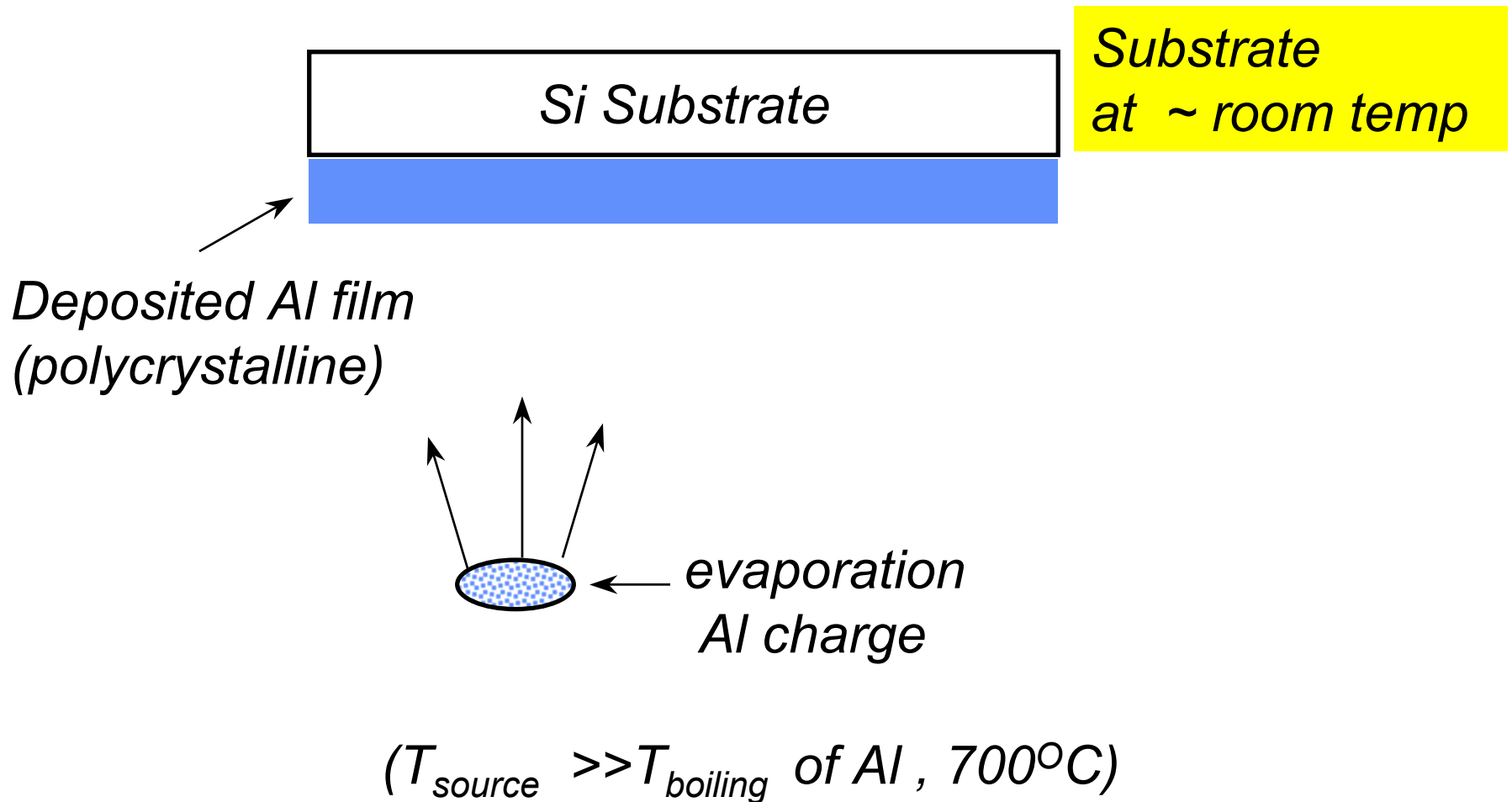
$$\left(\cong \sqrt{Dt} \right)$$



Concentration versus Depth

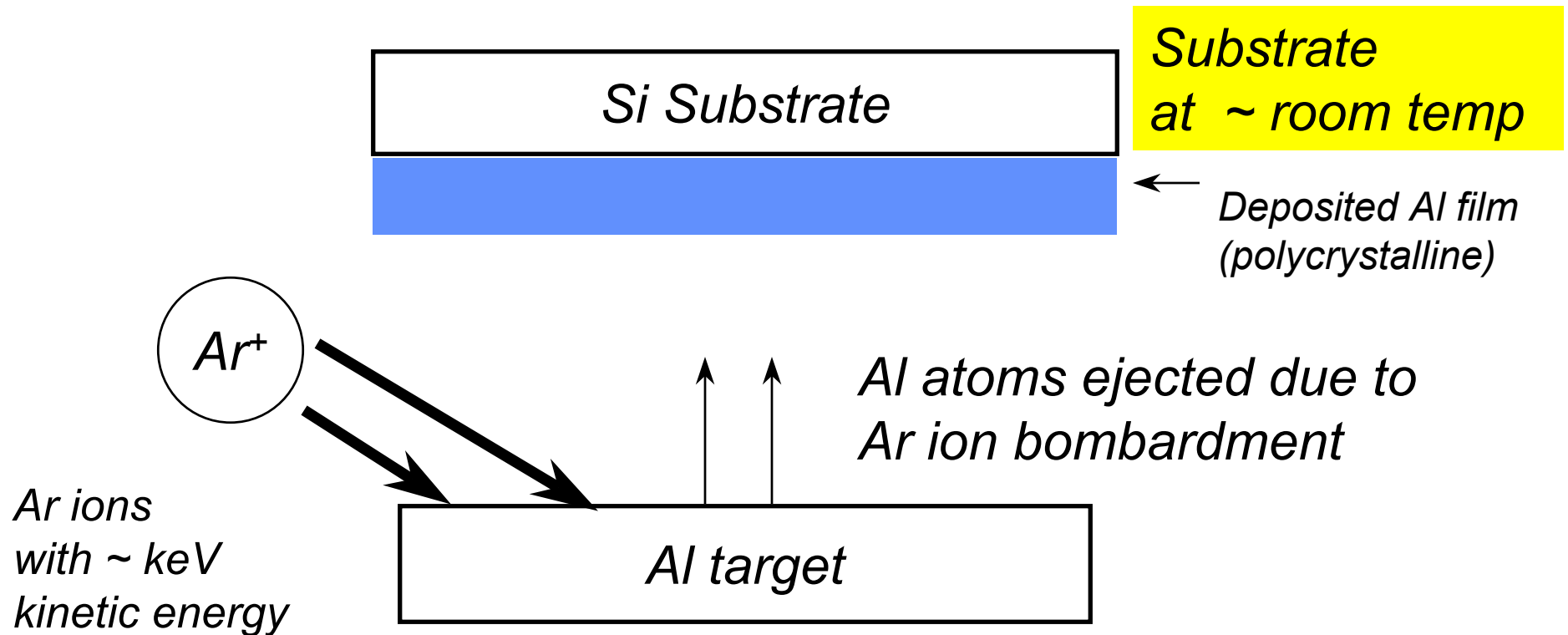
Physical Vapor Deposition (1)

Evaporation Deposition



Physical Vapor Deposition (2)

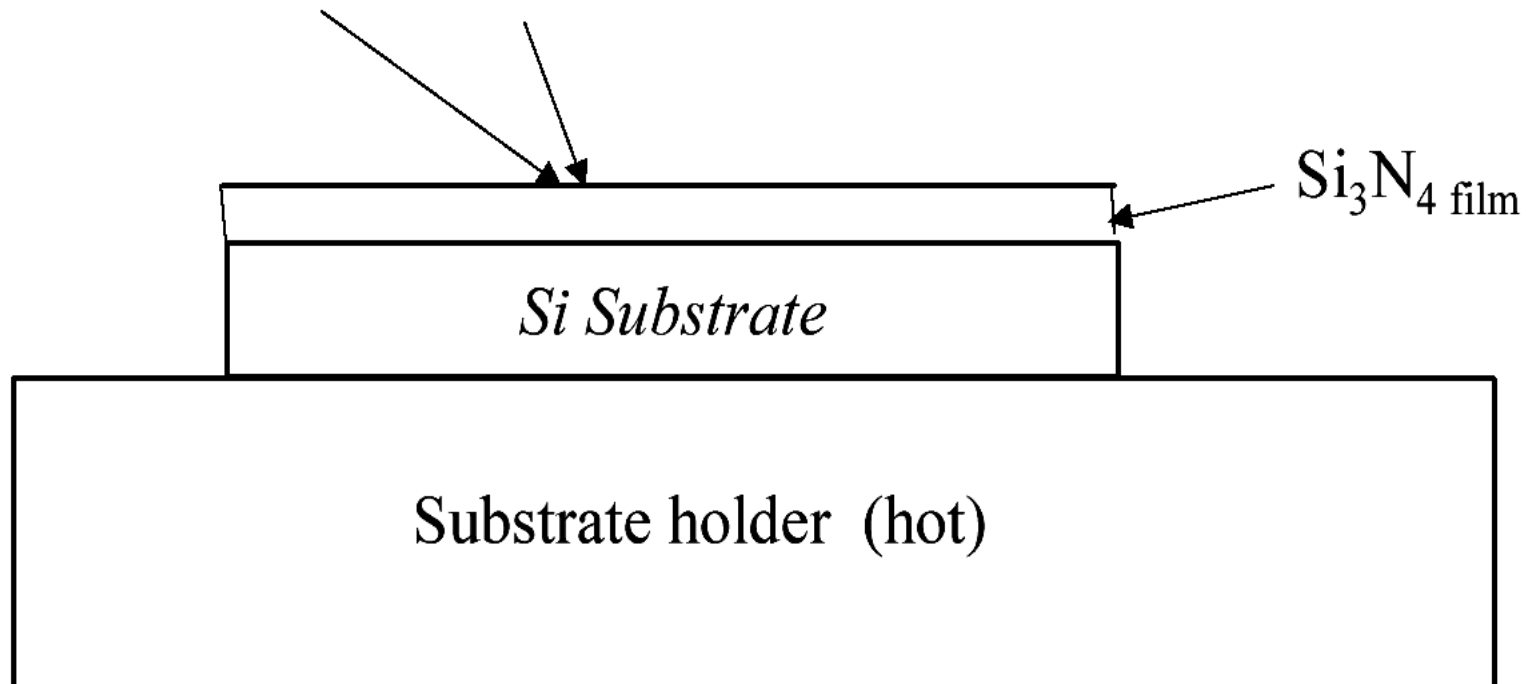
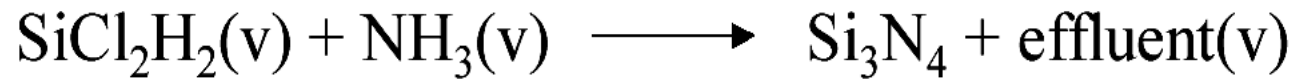
Sputtering Deposition



Chemical Vapor Deposition (CVD)

CVD, eg. of Si_3N_4

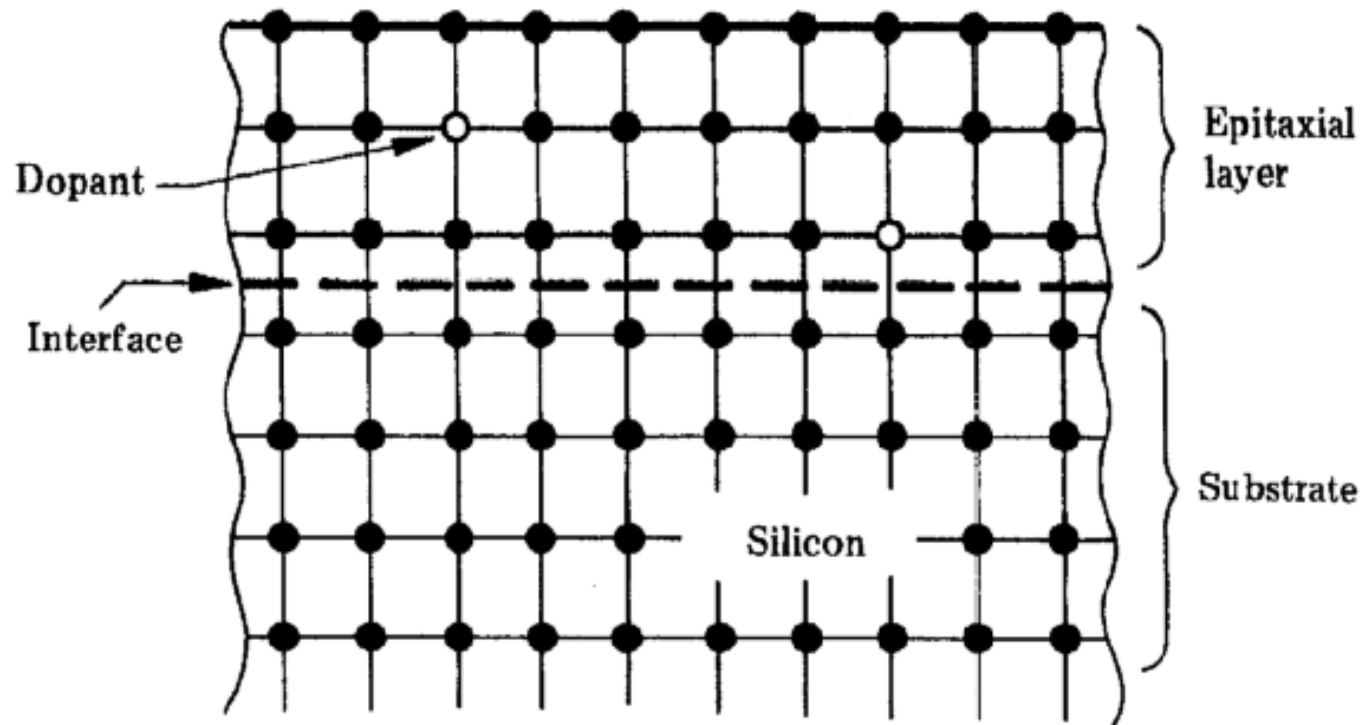
Processing Temperature
300-600°C



Solid films are formed by chemical reactions taking place at the surface.

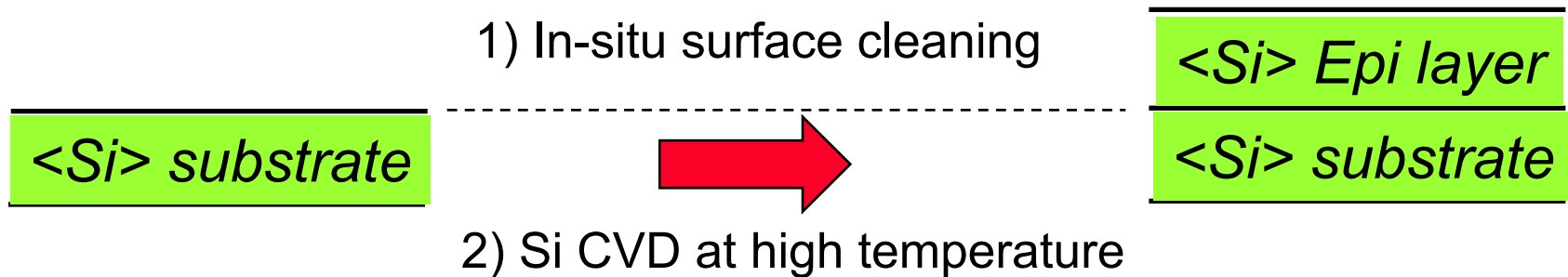
Epitaxial Growth

Processing Temperature
950-1150°C



- Requires an ultra-clean Si surface prior to epi growth.
- Requires deposition of Si at very high temperature for perfect crystallinity.

Epitaxial Growth



Typically used when we need a lightly doped single-crystal Si layer on top of heavily doped substrate.

Example

n^- <Si>	\updownarrow	$10^{15}/\text{cm}^3$
n^+ <Si> e.g. $10^{20}/\text{cm}^3$		

Cost of Silicon Real Estate

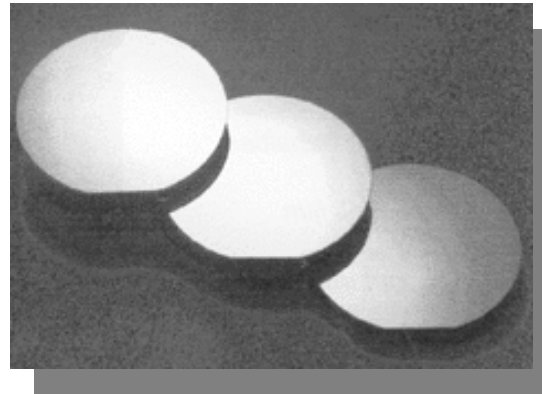
200mm Si wafer



\$80

$\$0.25 / \text{cm}^2$

200mm Epi wafer



\$140

$\$0.44 / \text{cm}^2$

1812 sq/ft House
Menlo Park, CA



\$944,492

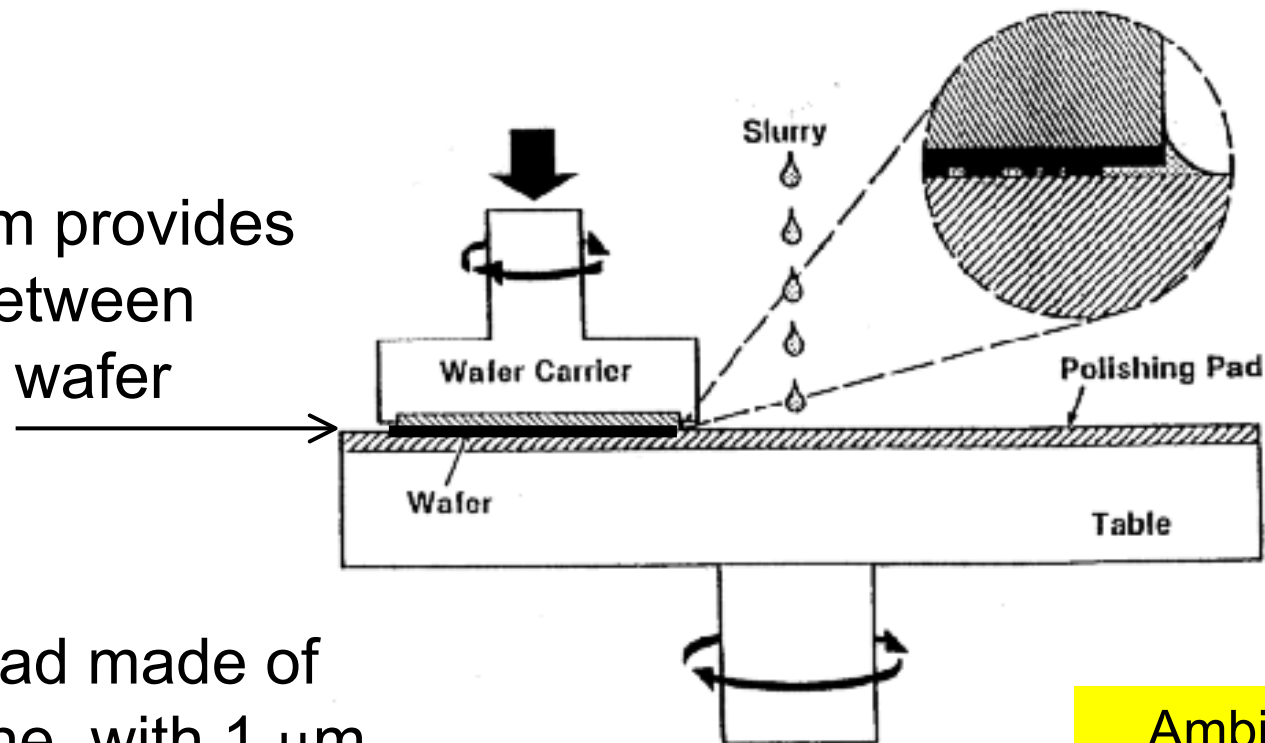
$\$0.56 / \text{cm}^2$

Chemical Mechanical Polishing (CMP)

Wafer is polished using a slurry containing

- silica abrasives (10-90 nm particle size)
- etching agents (e.g. dilute HF)

- Backing film provides elasticity between carrier and wafer
- Polishing pad made of polyurethane, with 1 μm perforations
 - rough surface to hold slurry



Ambient
Temperature

Metal Plating

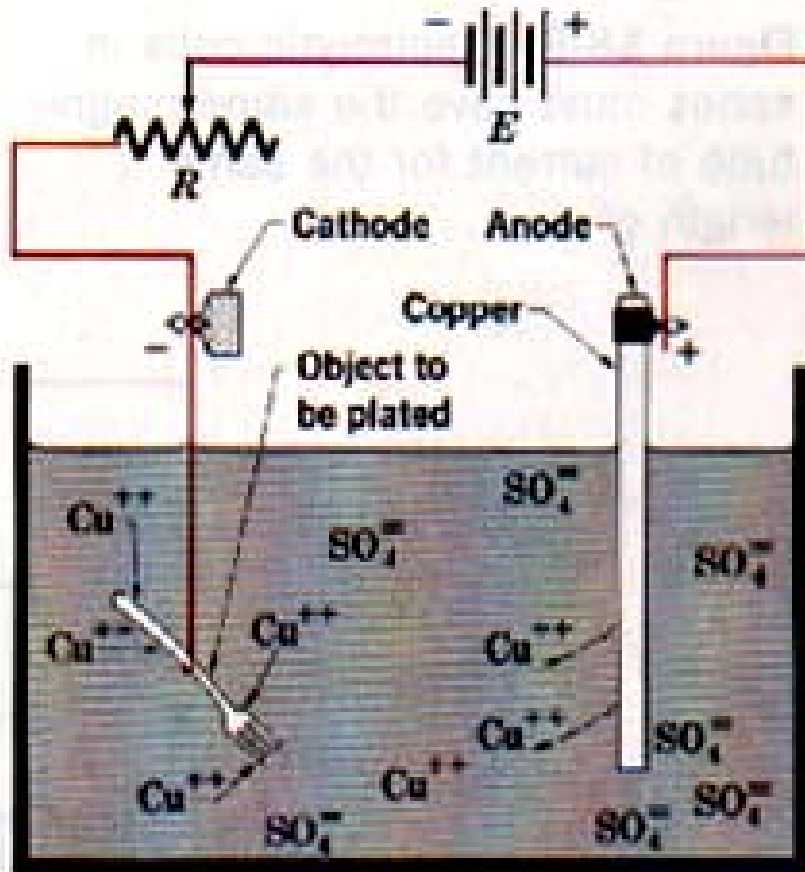
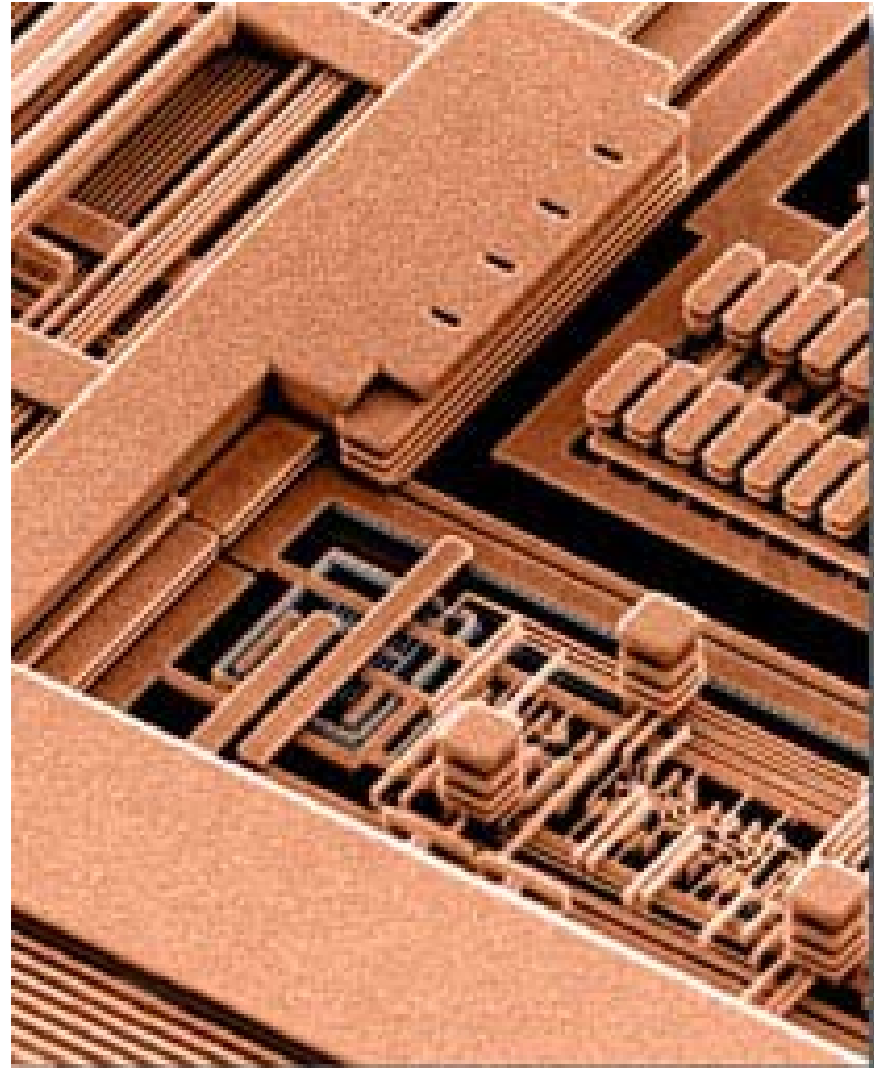


Figure 18-7. An electrolytic cell used for copper plating.

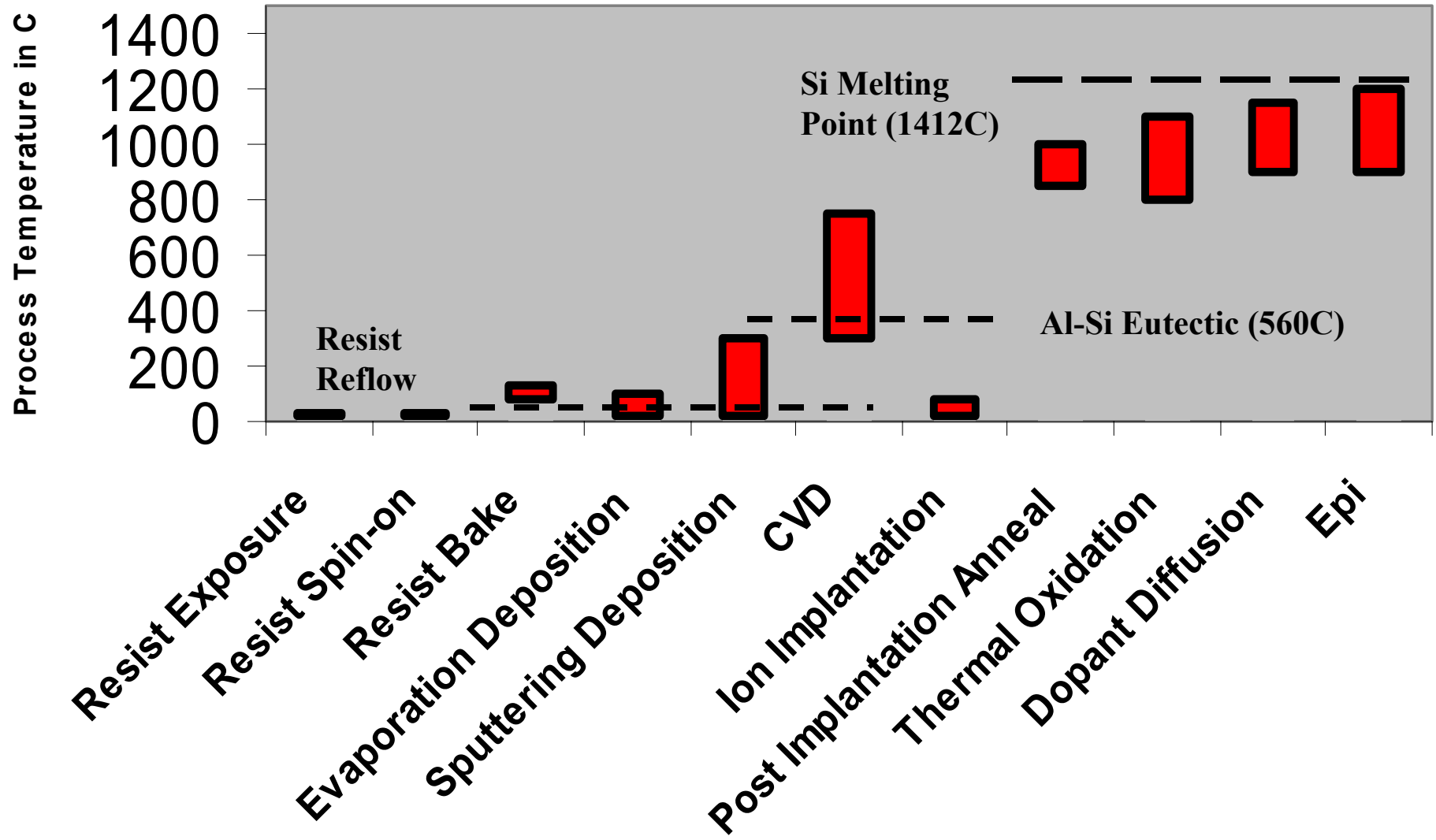
~ ambient temp



List of Conventional Microfabrication Modules

- Lithography
- Thermal Oxidation
- Etching (Chemical , Plasma)
- Ion Implantation
- Diffusion
- Physical Vapor Deposition PVD
- Chemical Vapor Deposition CVD and Epitaxial Growth
- Chemical Mechanical Polishing CMP
- Metal Plating

Processing Temperature and Material Failure Temperature



Interesting Facts about Chip Manufacturing

- **A typical 2-gram silicon chip requires 1.6 kilograms of fossil fuel, 72 grams of chemicals and 32 kilograms of water to manufacture.**
- To make the high-grade silicon needed for the chips requires 160 times the energy used to produce raw silicon. This accounts for about half of the total energy used by the chip. Only a quarter is consumed during its processing life.
- Because a chip's components are so tiny and precisely engineered, far more materials, such as fuels and solvents, are needed for their manufacture than for more traditional goods.
- The mass of these secondary materials outweighs the product by a factor of 600. In contrast, making a typical car requires only about twice its weight in fossil fuels.

Williams, E. D., Ayres, R. U. & Heller, M. The 1-7 kilogram microchip: energy and material use in the production of semiconductor devices. *Environmental Science and Technology*, Published online (2002).