# EE143 General Information

**Instructor** : Prof. Nathan Cheung , Cory 513, 642-1615,
cheung@eecs.berkeley.edu
**Lecture Hours and Place**: Tu &Th, 9:40-11:00am, Etcheverry 3106
**Office Hours**: Tu 12-2pm, W 1-2pm, and by appointment via e-mail

**Required Text :**
1) R.C. Jaeger "Introduction To Microelectronics Fabrication ", 2nd Edition
2) EE143 Reader (if you have S2005 version, no need to buy the F2005 version)

**Homework**: Weekly homework assignments due on Thursdays.

**Grading**: Midterm1 15%,Midterm2 15%, Final 30% ,Homework 10%, Lab 30%
(undergrad and grad will be graded as two separate groups)

***Browse last semester's course content for lecture notes, homework, and exams. http://www-inst.eecs.berkeley.edu/~ee143/sp05index.html

## Lab Sign-up required for ALL students

## 6 Lab Sections : M2-5pm, W 9-12am, W 2-5pm, Th 2-5pm, Fri 9-12am, Fri 2-5pm

- Sign-up sheets will be posted outside Cory 218 after 11am (8/31, Tue) .You have to sign up personally at Cory 218 before 5pm (9/1,Thur) even you are enrolled by Telebear. If you do not do so, your name will be removed from the class list
- Final lab assignment will be posted outside Cory 218 and on class webpage on 9/2(Friday).
- Assignment priority : (1) Telebear enrolled, (2) Telebear waitlist , (3) No Telebear enrollment. Order of sign-up not important.
- NO Lab Meeting the week of 8/29

## Week of 9/5

**Mandatory Lab attendance required.**

- **You will have lab orientation and have to pass a safety quiz.**

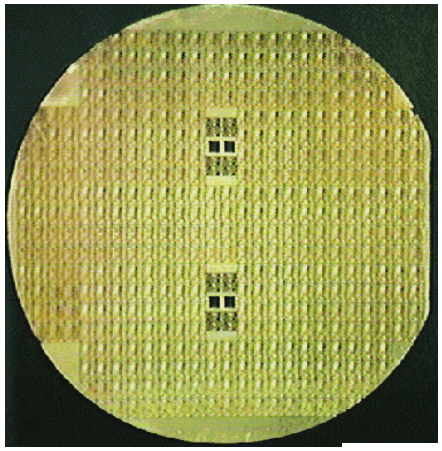
- **Because of Labor Day Holiday, there will be no Monday afternoon lab section. Students assigned to that section can attend any of the other 5 sections (only for this week).**

**Lectures, HW, Lab Info, and News (check regularly)**
http://www-inst.eecs.berkeley.edu/~ee143/

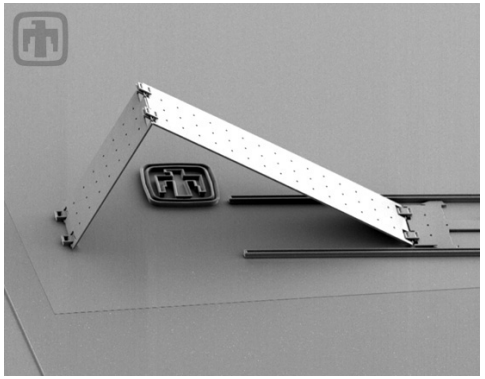
## Other Websites for EE143 Overview

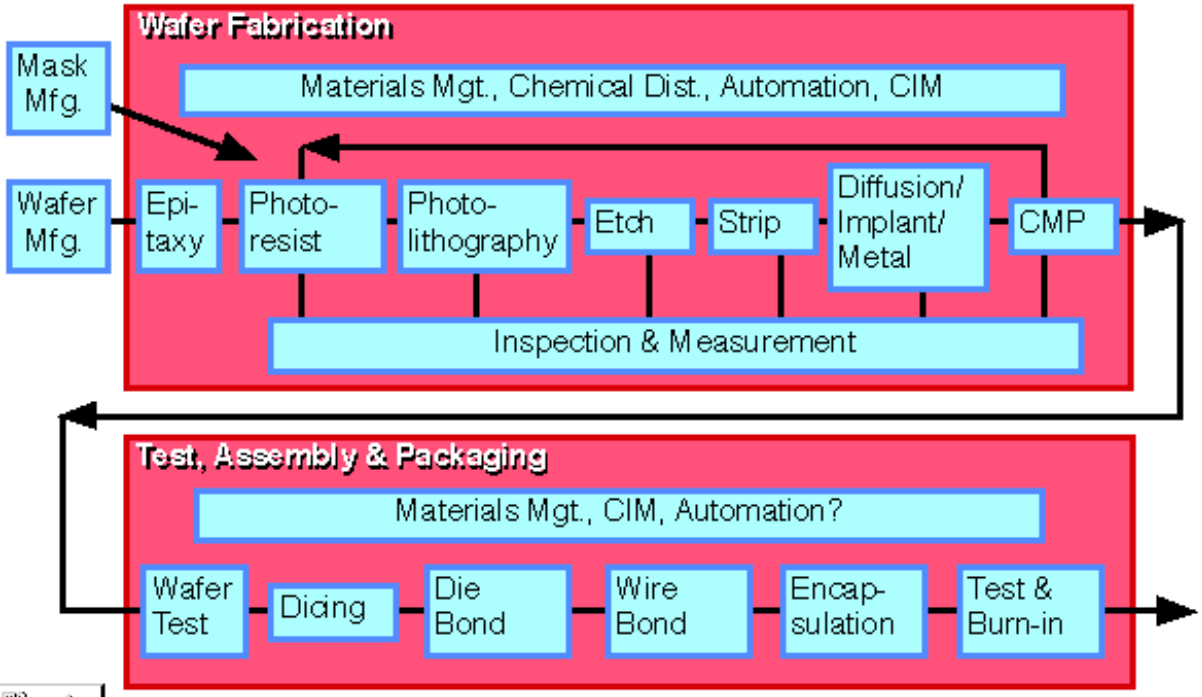
**Device Physics/ Process Visualization – Highly recommended**
(Change the device parameters and watch the resultant
space charge, energy bands , I-V , C-V etc)
**http://jas.eng.buffalo.edu/**
**MEMS operation (Good collection of photos and movies)**
**http://mems.sandia.gov/scripts/index.asp**
**SIA Roadmap (Trend and Challenge)**
http://public.itrs.net/
**EE Basics (E40 course material)**
http://www-inst.eecs.berkeley.edu/~ee40/
**Trends and forecast**
www.icknowledge/com

# What is EE143 all about?



- **Microfabrication Principles for IC and MEMS**
- **Hands-on Fabrication and Testing of IC and MEMS Devices**

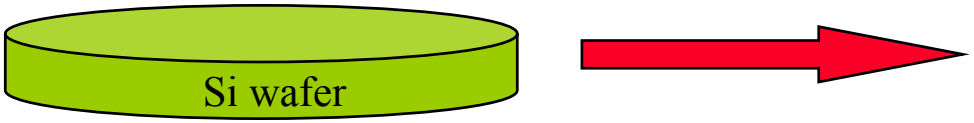




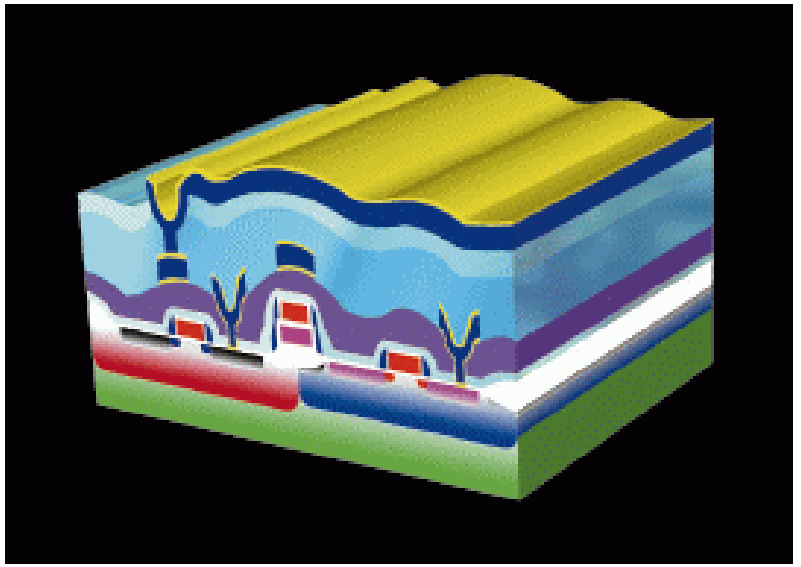
# Principle of Monolithic Process Integration

* A sequence of ***Additive*** and ***Subtractive*** steps with **lateral patterning**

Example: CMOS Integrated Circuit

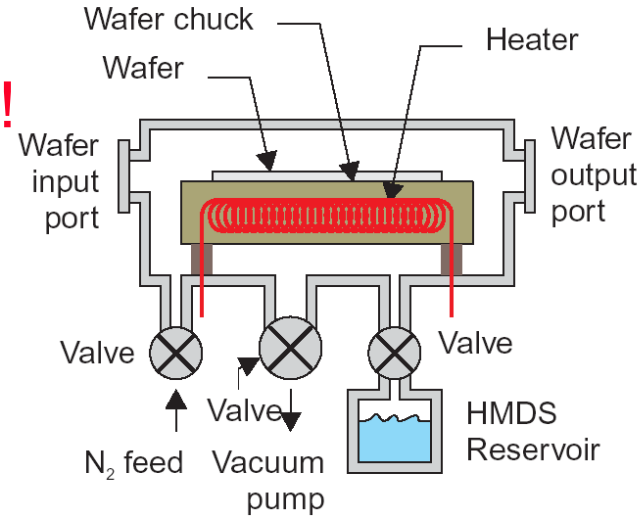



Processing Steps

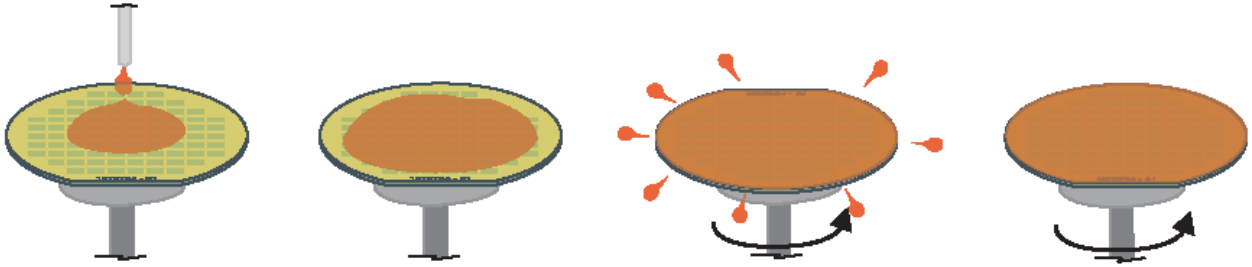


# A Process Module has many sub-steps!

Example : Deep UV Photolithography




**1) Surface Prime**



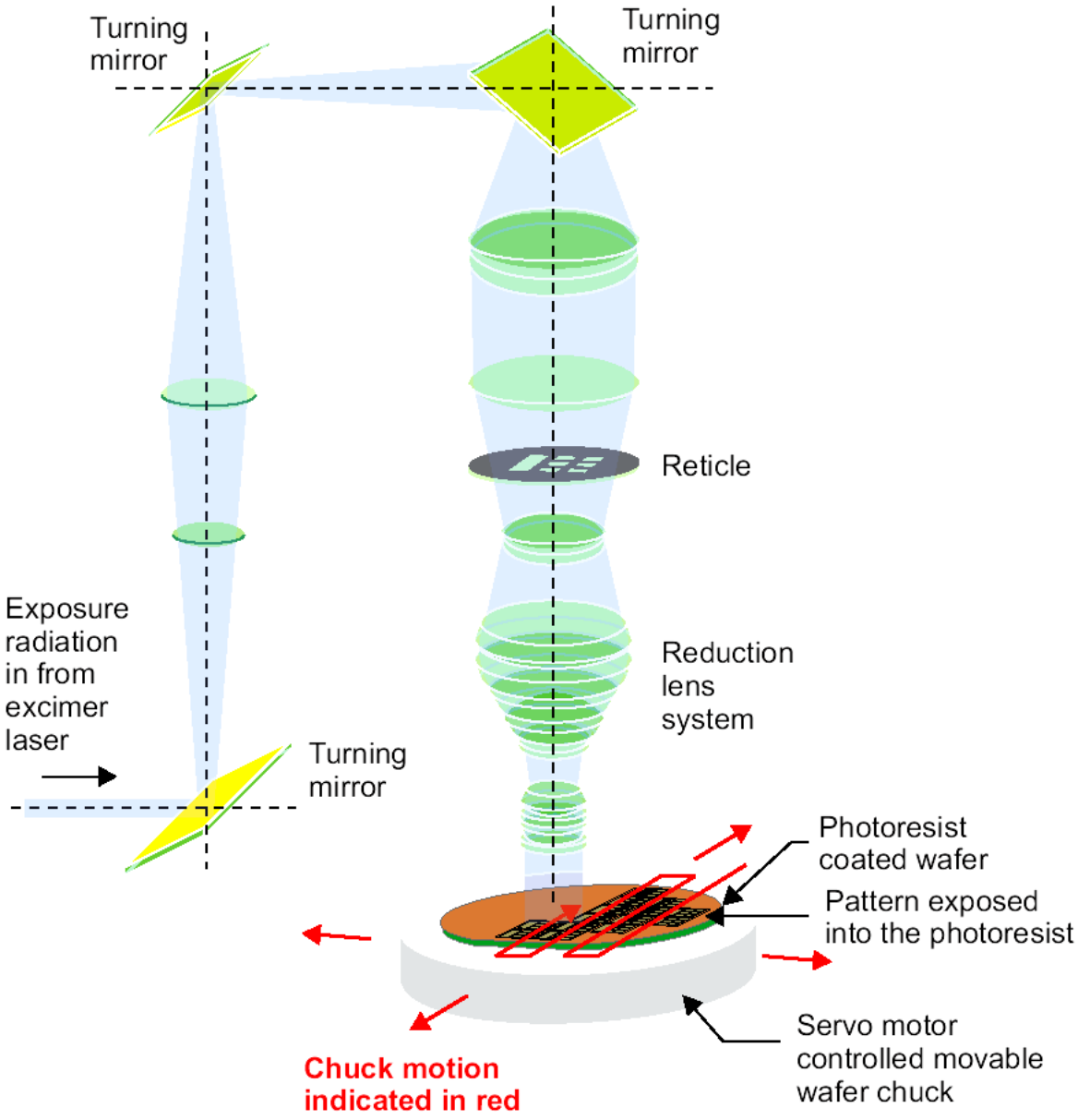
Dispense a controlled amount of photoresist

Allow the photoresist to spread across the wafer

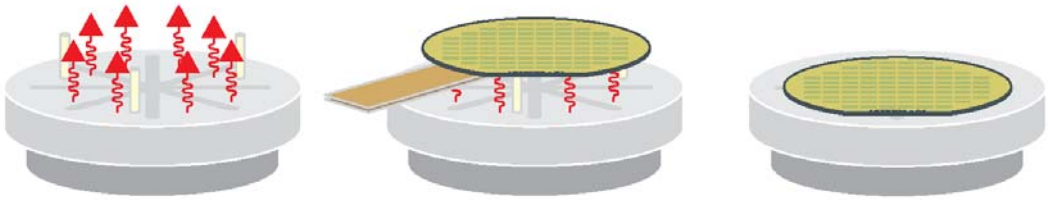
Rapidly ramp - up the coater spin speed throwing off excess photoresist

Spin at high speed to form a thin dry film of photoresist

**2) Coat**


Turning mirror
Turning mirror
Reticle
Exposure radiation in from excimer laser
Turning mirror
Reduction lens system
Photoresist coated wafer
Pattern exposed into the photoresist
Servo motor controlled movable wafer chuck
Chuck motion indicated in red

**4) Expose**

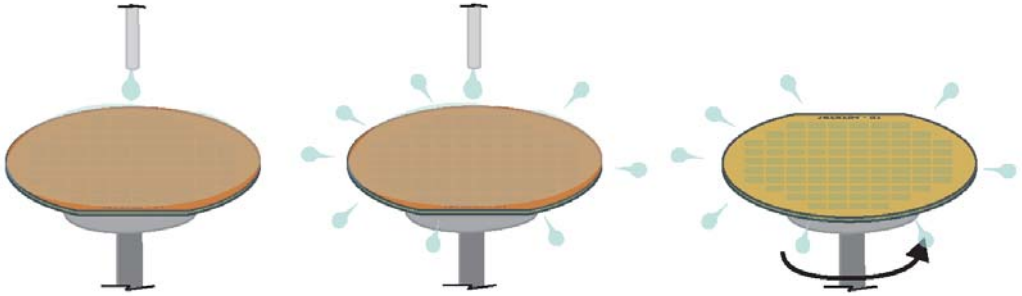


Hot chuck with lift pins "up"

Wafer loaded onto lift pins

Lift pins down, wafer is baking

**3) Pre-bake**
**5) Post Exposure Bake**
**7) Hard Bake**



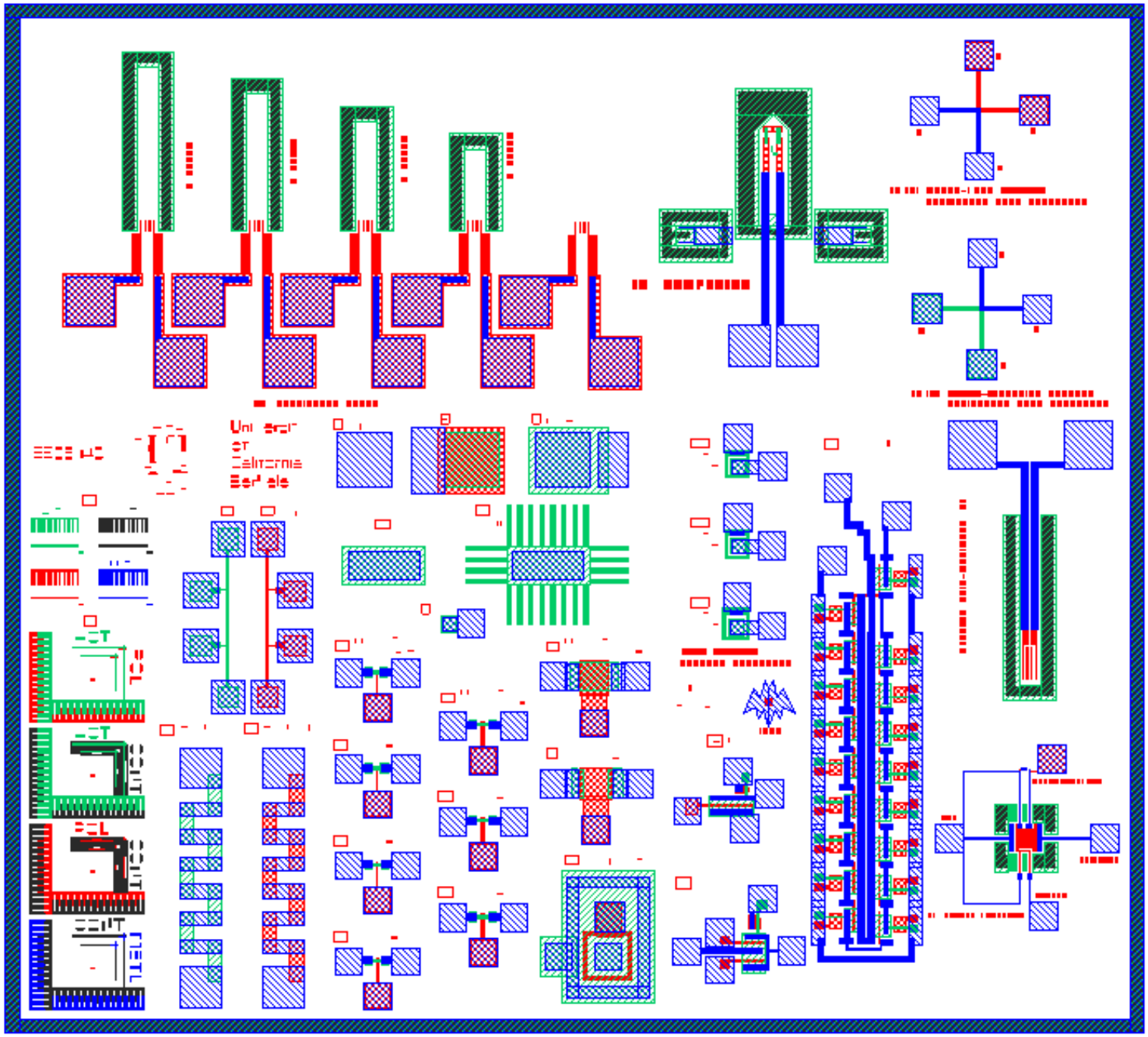
Dispence a puddle of developer and allow it to sit.

Dispence a rinse solution while slowly spinning the wafer.

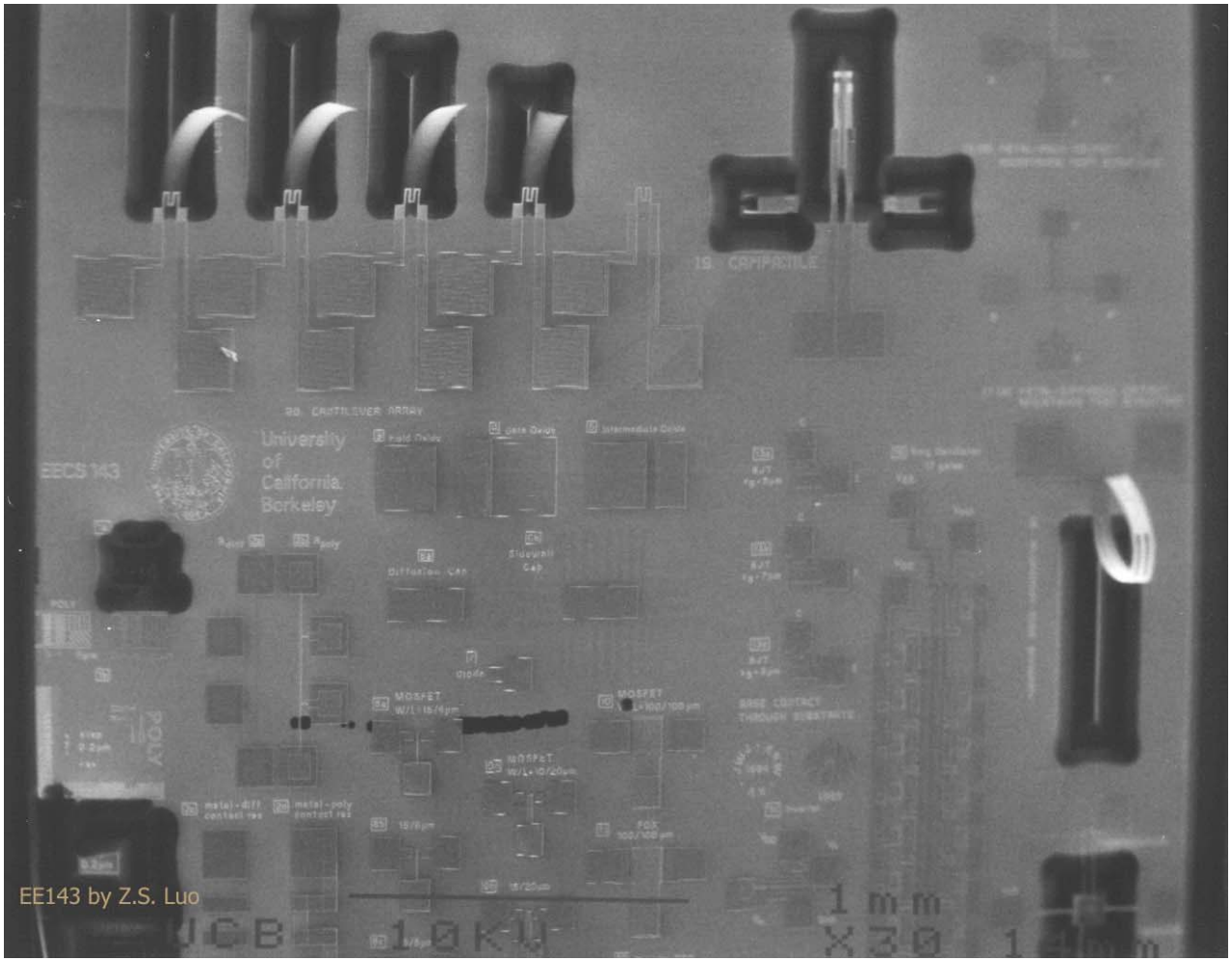
Ramp up to high speed and spin the wafer dry.

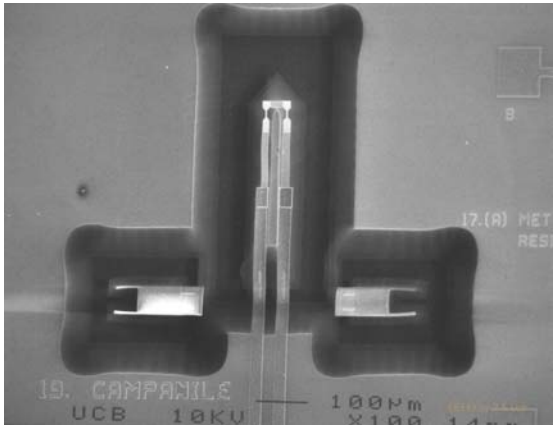
**6) Develop**

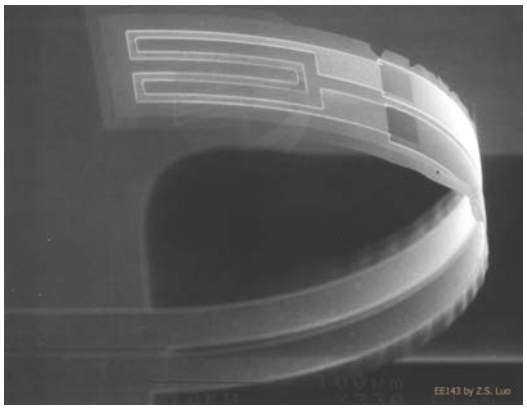
# EE143 Chip Fabrication

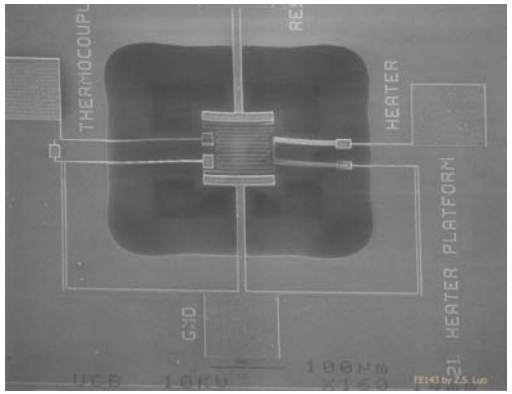


# SEM Micrographs of EE143 Chip

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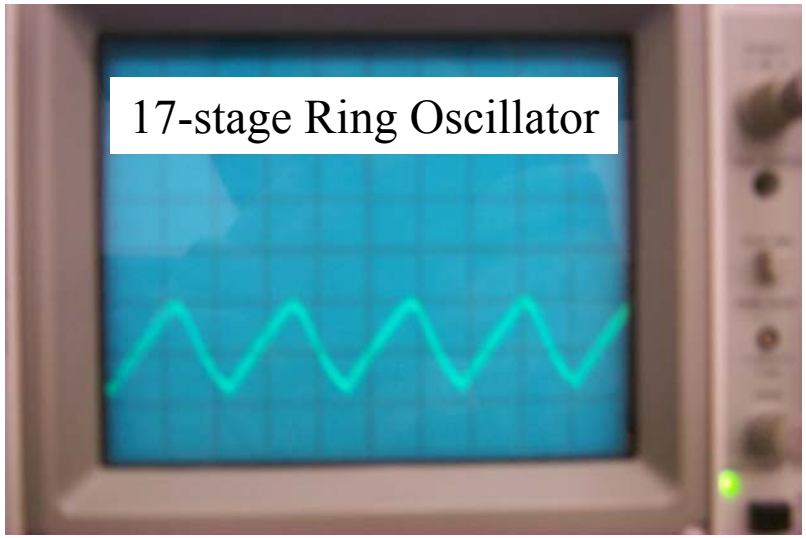
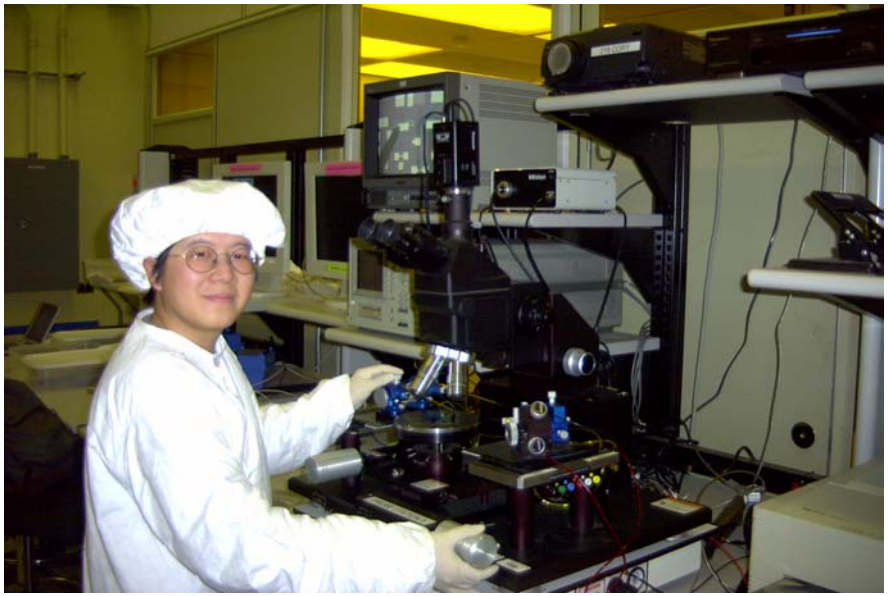
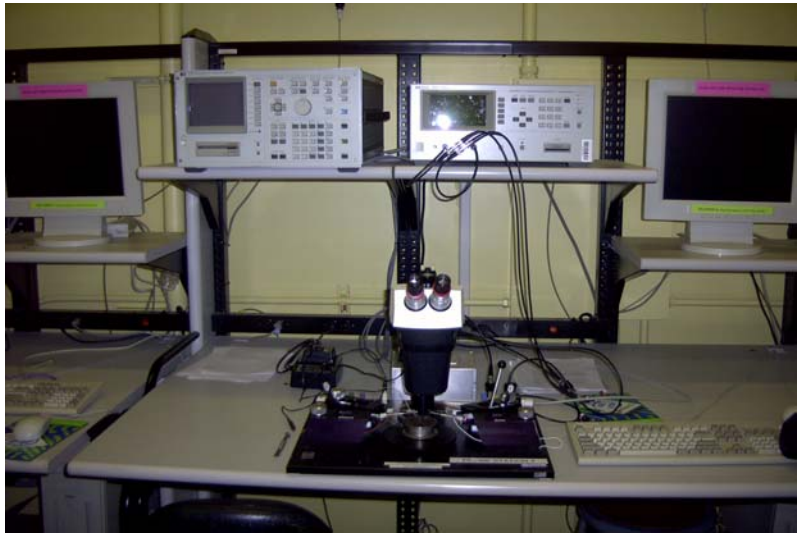
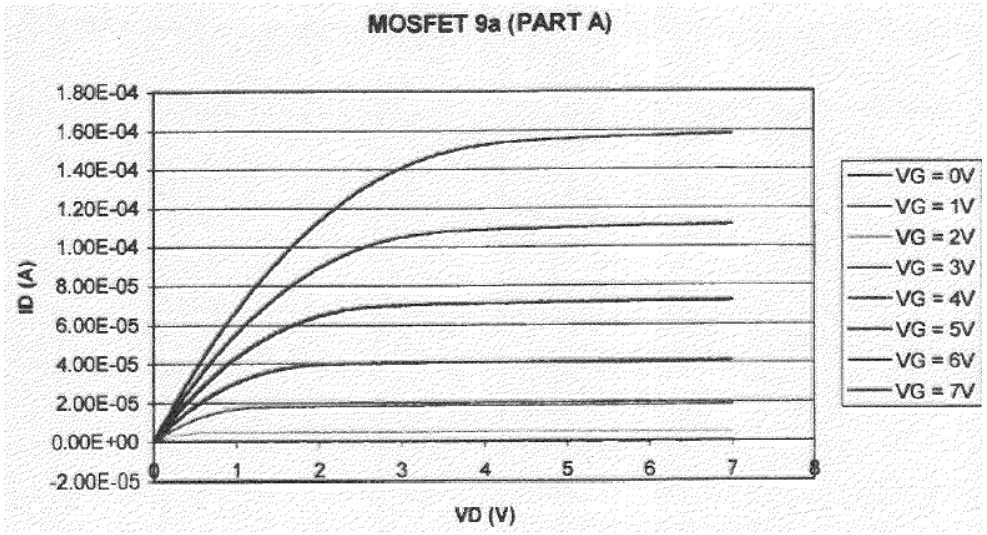
# EE143 Chip Characterization



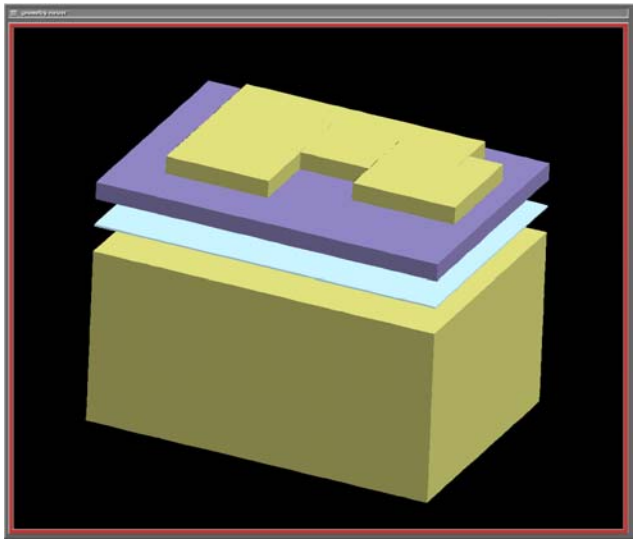




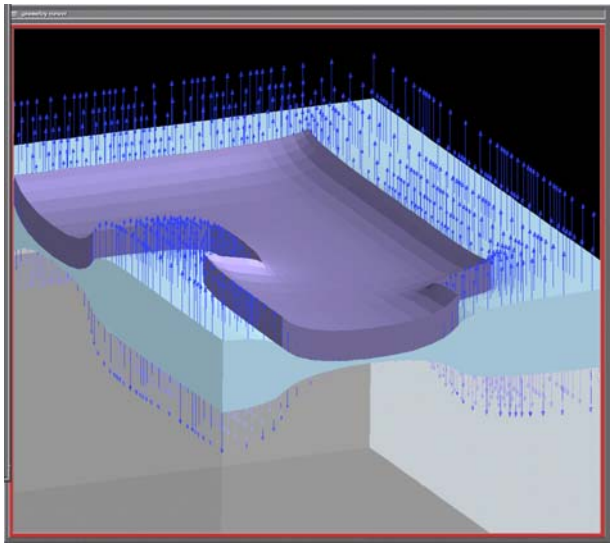
# Process Simulation

**** 3D Topography and Dopant Distribution***

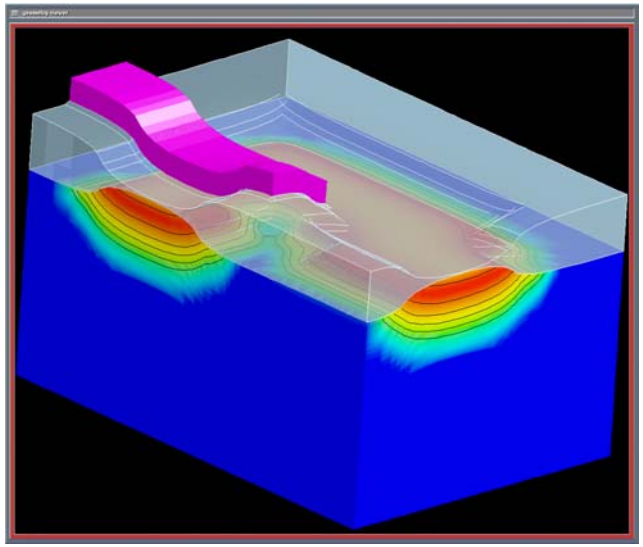
After resist patterning on nitride/pad oxide



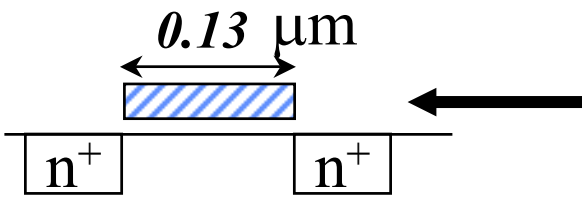
After Local Oxidation



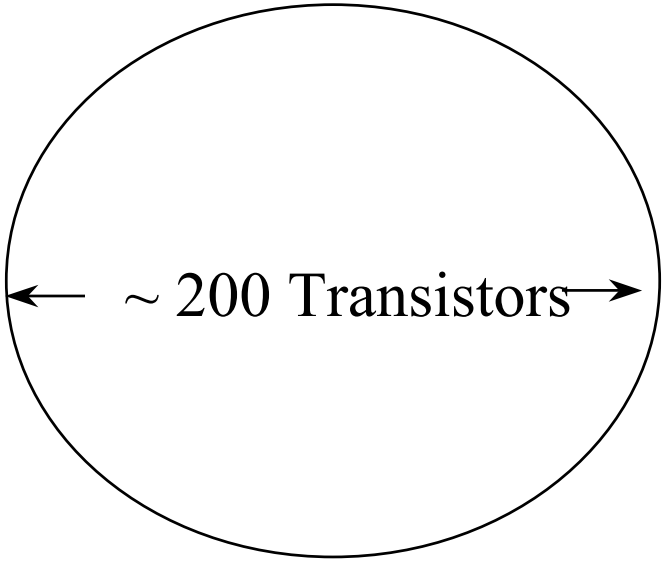
After Poly-Si Gate Patterning



$1\mu m = 10^{-4}\,cm = 10^{-6}\,m = 1000\,nm$



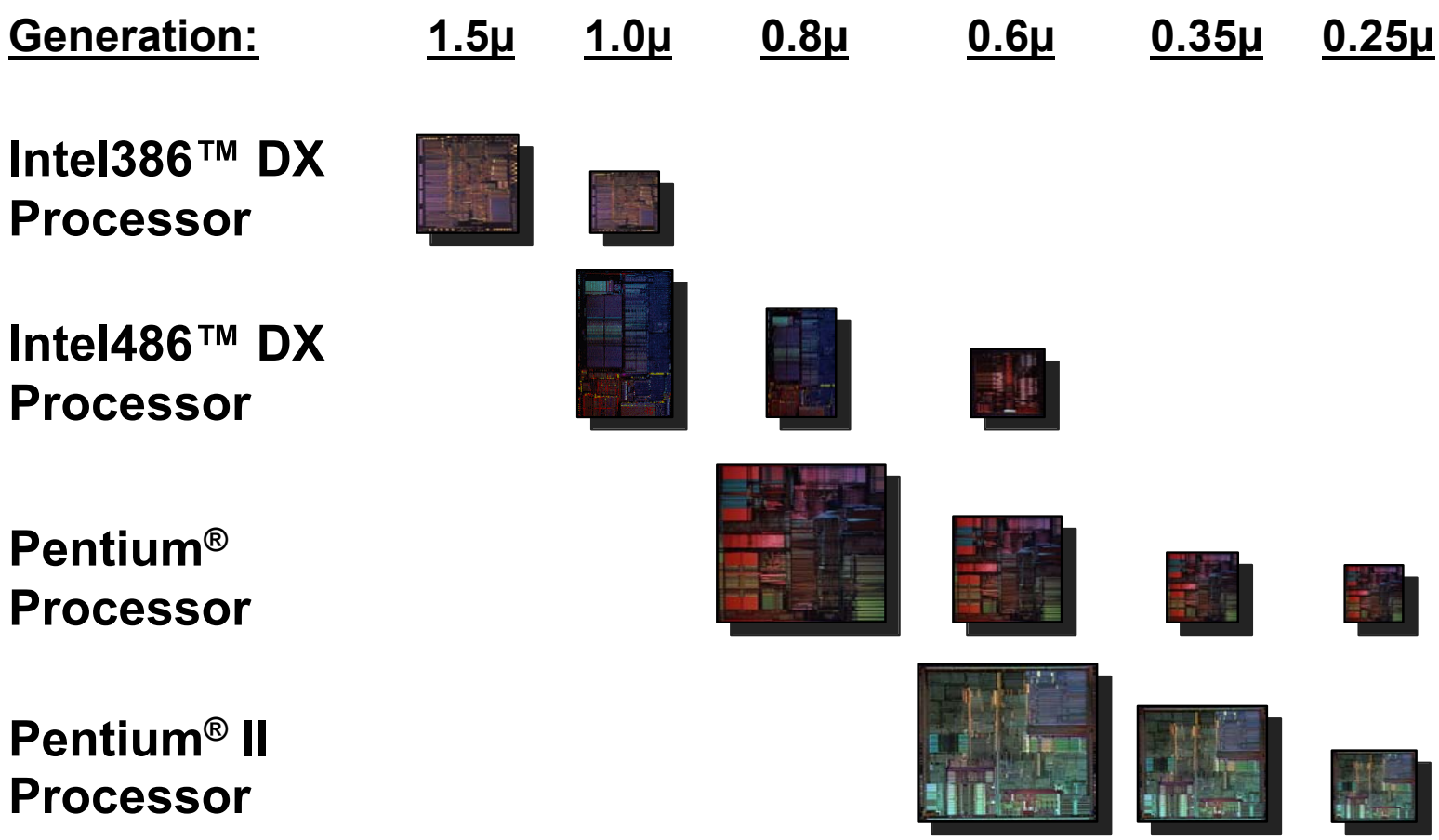

State-of-the-art Mass Production IC




Diameter of human hair ~50μm

# Advantages of Technology Scaling

- More dies per wafer, lower cost
- Higher-speed devices and circuits ( electrical signals travel shorter distances)



# The beauty of silicon

For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by

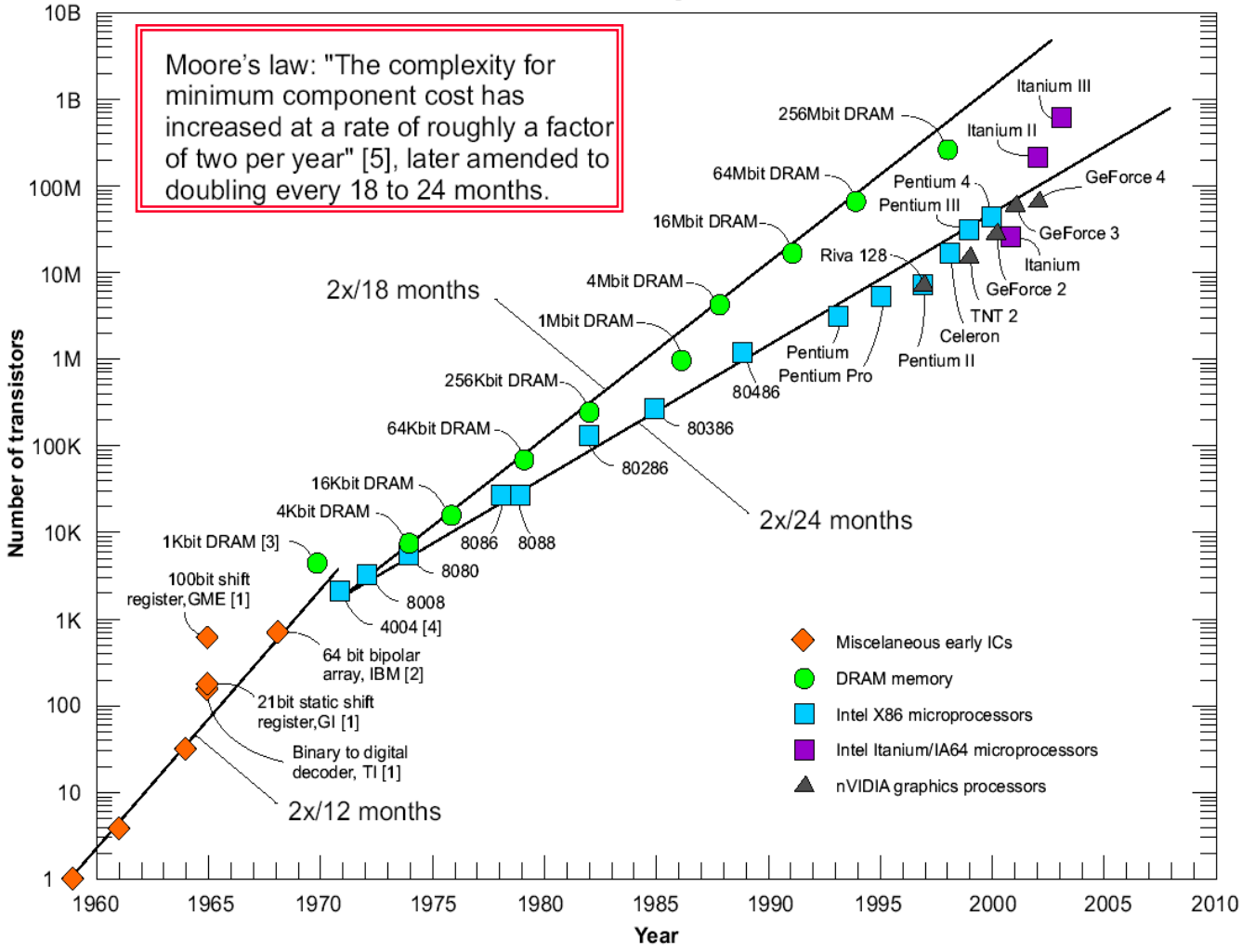
SCALING

1. Scaling device dimensions downward
2. Scaling wafer diameter upward

| | 1990 | 1995 | 2000 |
|---|---|---|---|
| DRAMs | 4 MB | 64 MB | 1 GB |
| Feature size | 0.8 µm | 0.35 µm | 0.15 µm |
| Wafer diameter | 6” | 8” | 12” |
| Cost per Megabit | $6.50 | $3.14 | $0.10 |

# Transistor Per Integrated Circuit Trends

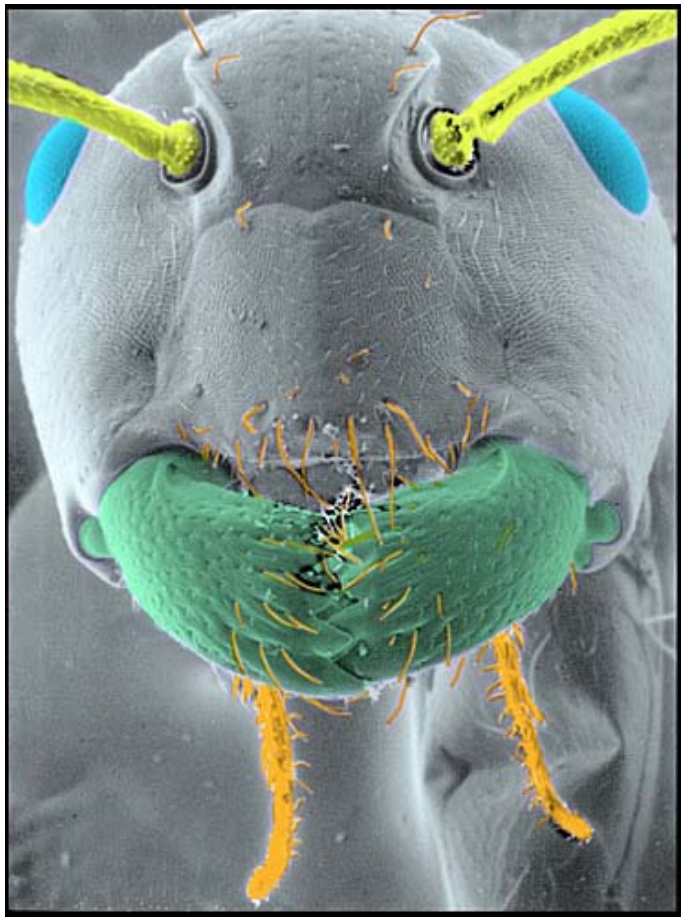
www.icknowledge.com





[1] Stanley Mazor, "The History of the Microcomputer - Invention and Evolution" http://www.dotpoint.com/xnumber/Microcomputer_invention.htm.
[2] Bob Donlan and David Pricer, "Pushing the Limits: Looking Forward...Looking Back," Microelectronic Design, Vol. 1., (1987).
[3] "Inventions of the Modern Computer: Intel 1103 The World's First Available DRAM Chip," http://inventors.about.com/science/inventors/library/weekly/aa100898.htm.
[4] Jonathan Cassell, "Who Really Invented the Microprocessor," http://www.ebnonline.com/25year/25_microprocessor2.html.
[5] Gordon E. Moore, "Cramming more components onto integrated circuits," Electronics, Vol. 38, N. 8, Apr. (1965).

# *Another Perspective on Moore's Law*



… we are already producing $10^{18}$ transistors per year. Enough to supply every ant on the planet with ten transistors.

Twenty years from now, if the trend continues, there will be more transistors than there will be cells in the total number of human bodies on Earth.

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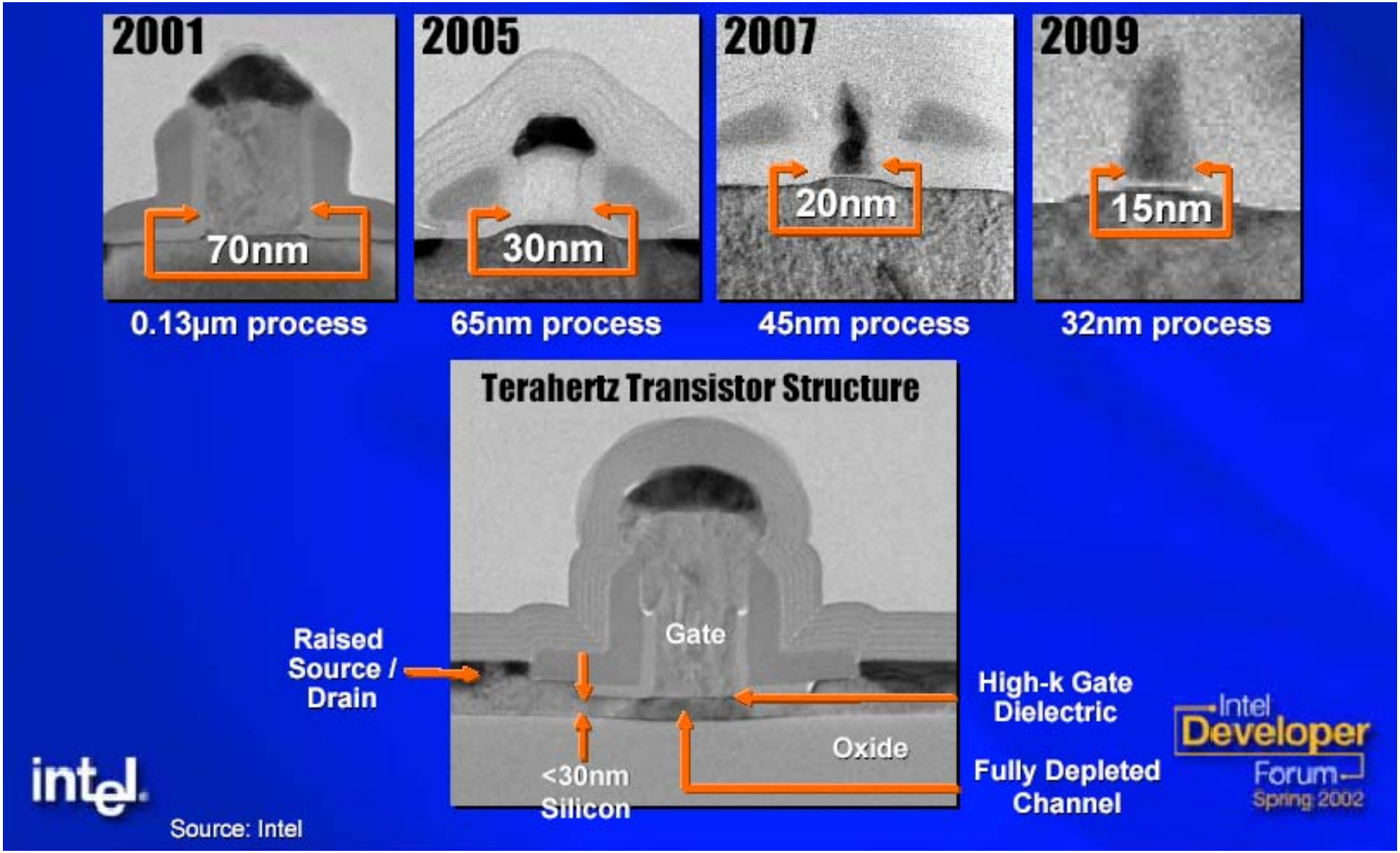
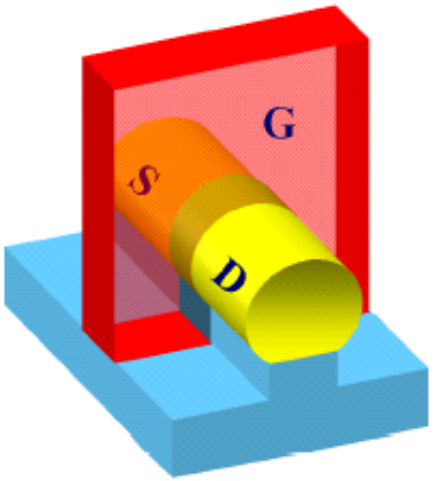
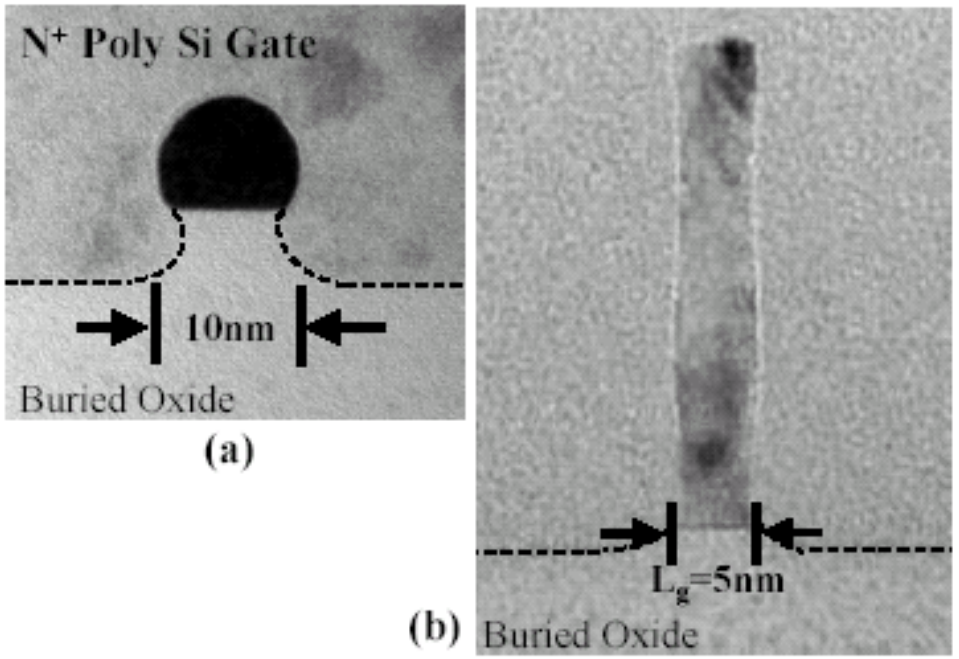

2001
70nm
0.13µm process
2005
30nm
65nm process
2007
20nm
45nm process
2009
15nm
32nm process
Terahertz Transistor Structure
Raised Source / Drain
Gate
High-k Gate Dielectric
Oxide
<30nm Silicon
Fully Depleted Channel
Source: Intel
intel
Intel Developer Forum Spring 2002

# 5nm-Gate Nanowire FinFET




Nanowire
FinFET
($T_{si} = 2L_g$)




2004 Symposium on VLSI Technology, p.196

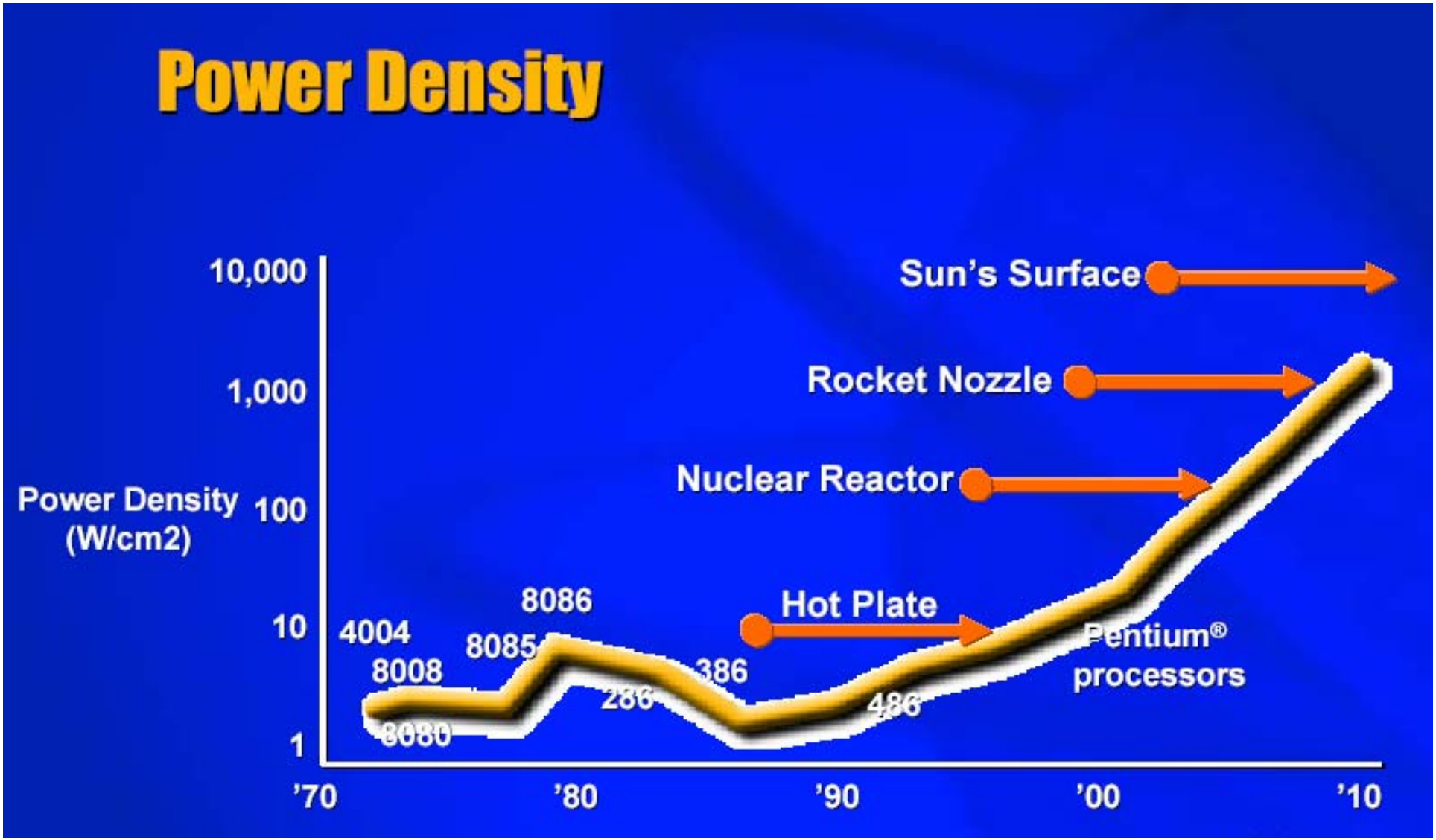
# SIA roadmap

http://public.itrs.net/

## Memory and Logic Technology Requirements

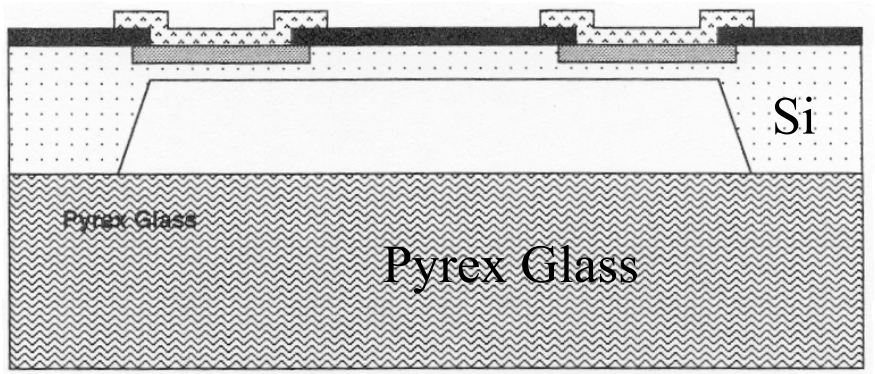
| *Year of First Product Shipment Technology Generation* | *1999 180nm* | *2001 150nm* | *2003 130nm* | *2006 100nm* | *2009 70nm* | *2012 50nm* |
|---|---|---|---|---|---|---|
| *Min. Logic $V_{dd}$ (V)* | **1.8-1.5** | **1.5-1.2** | **1.5-1.2** | **1.2-0.9** | **0.9-0.6** | **0.6-0.5** |
| *$T_{ox}$ Equivalent (nm)* | **3-4** | **2-3** | **2-3** | **1.5-2** | **<1.5** | **<1.0** |
| *Equivalent Maximum E-field (MV/cm)* | **5** | **5** | **5** | **>5** | **>5** | **>5** |
| *Nominal $I_{on}$ @ 25°C (μA/μm) (NMOS/PMOS)* | **600/280** | **600/280** | **600/280** | **600/280** | **600/280** | **600/280** |
| *S/D Extension Junction Depth, Nominal (nm)* | **36-72** | **30-60** | **26-52** | **20-40** | **15-30** | **10-20** |

## Chip Power consumption is a big concern !!!!



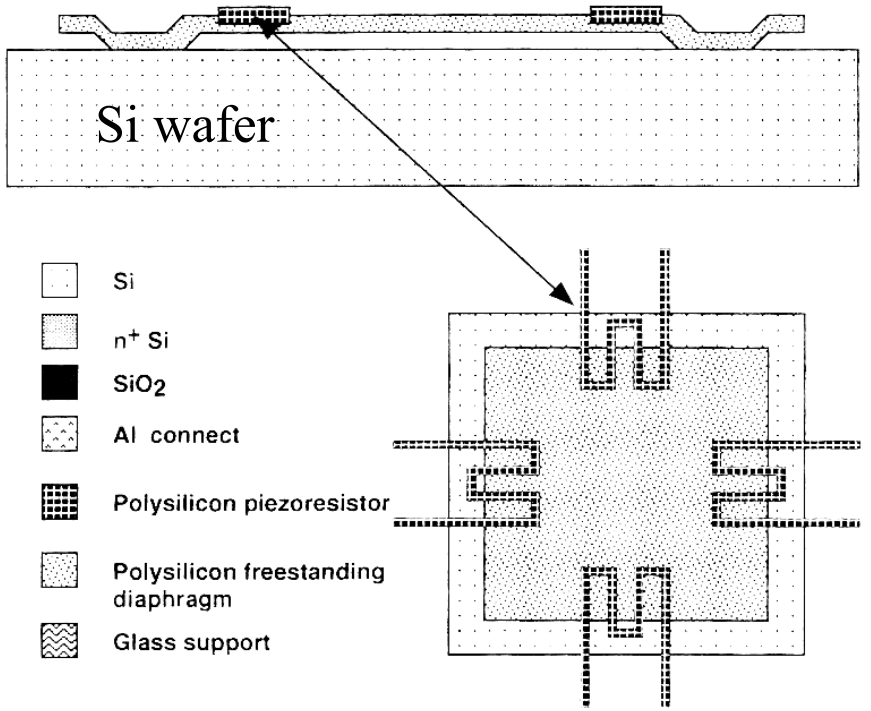

Source: Intel Developer Forum 2002

# MEMS: Pressure Transducer

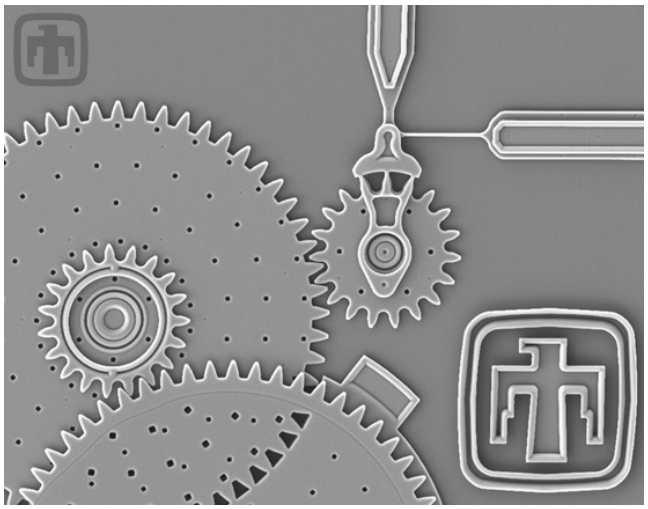



***Bulk Micromachining***

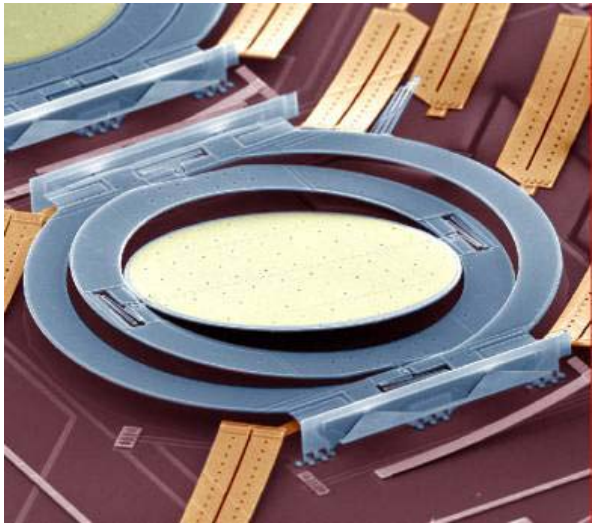
***Surface Micromachining***



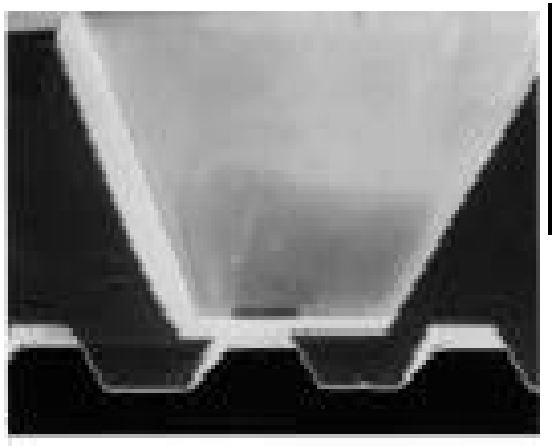
# MEMS Actuators



**Gear Speed Reduction Unit**



**Movable Mirror**



**Responsive Drug Delivery Valve**

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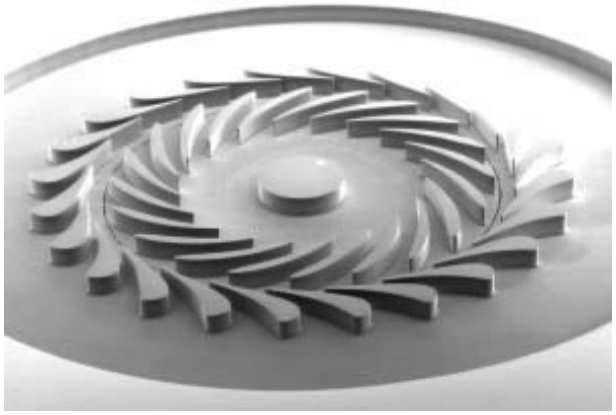
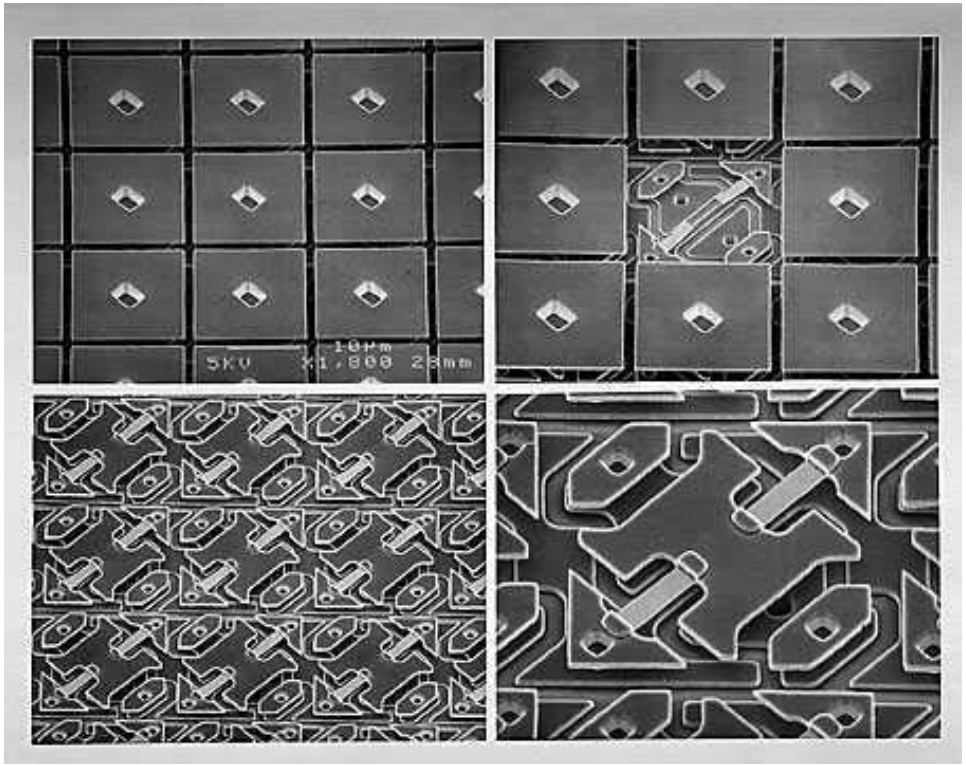


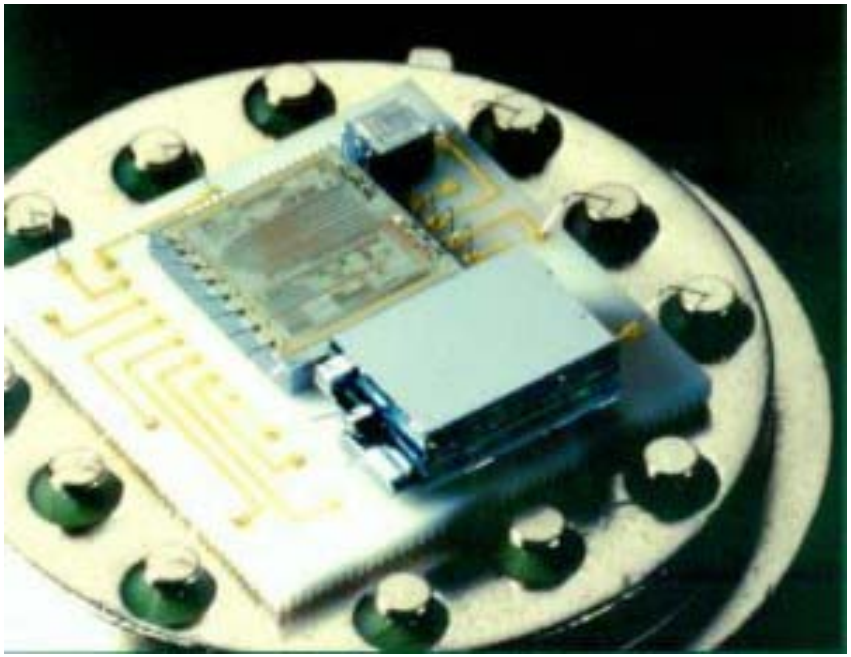
**Turbine engine**

# Commercial MEMS Products

- Optomechanical Displays (TI, 1996)

•Acceleratometer ( Analog Devices)

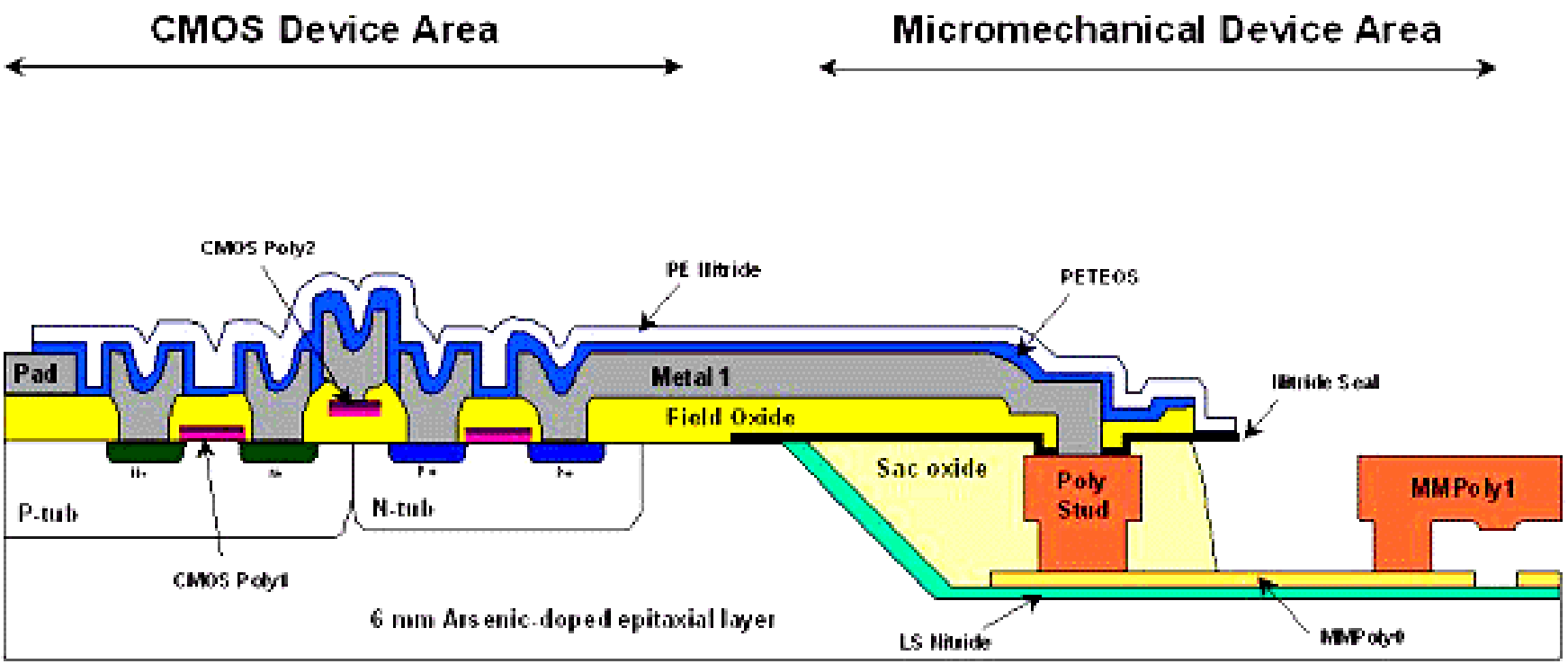




# MEMS-IC Integration

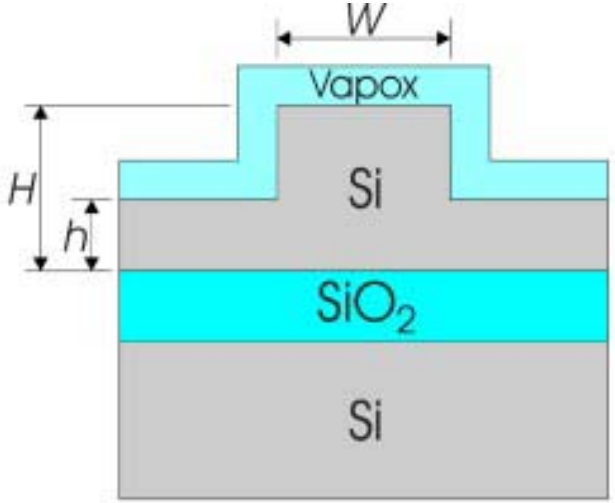
(Sandia National Lab)

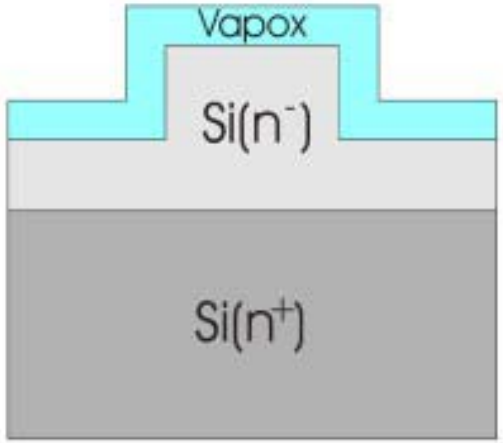
- MEMS fabricated in 12μm-deep trench
  - Filled with $SiO_2$ and planarized using CMP

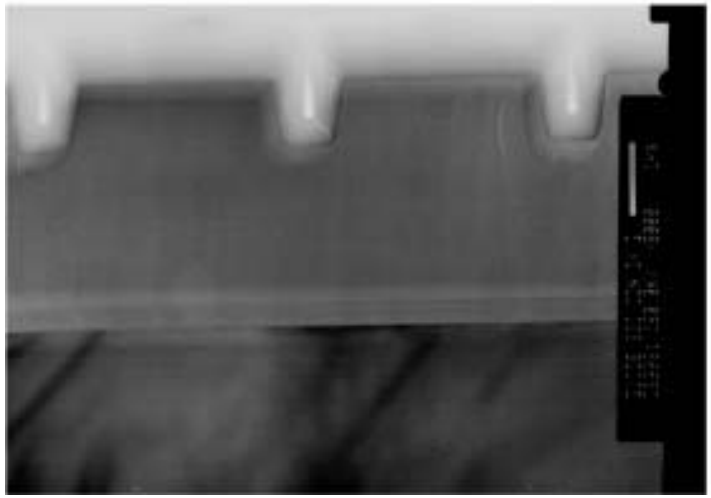


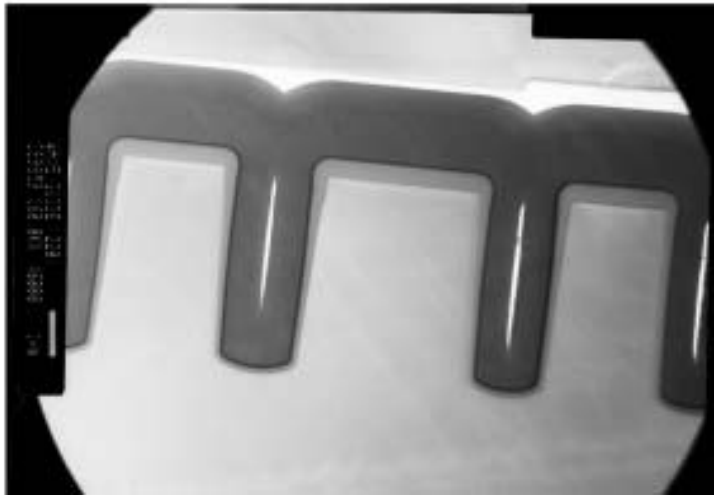
# Silicon-COmpatible OPtoelectronics (SCOOP)

## Si-BASED WAVEGUIDES

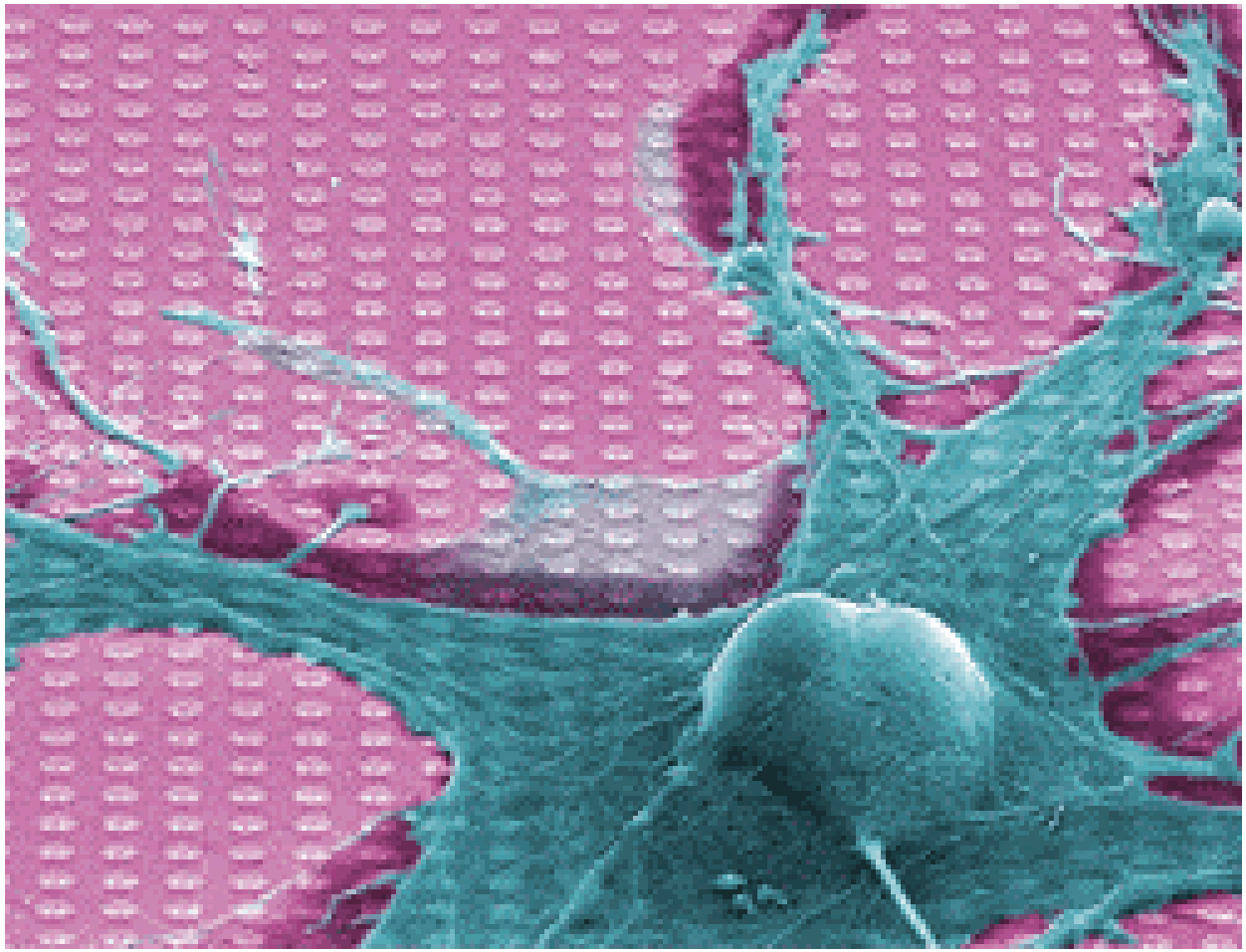




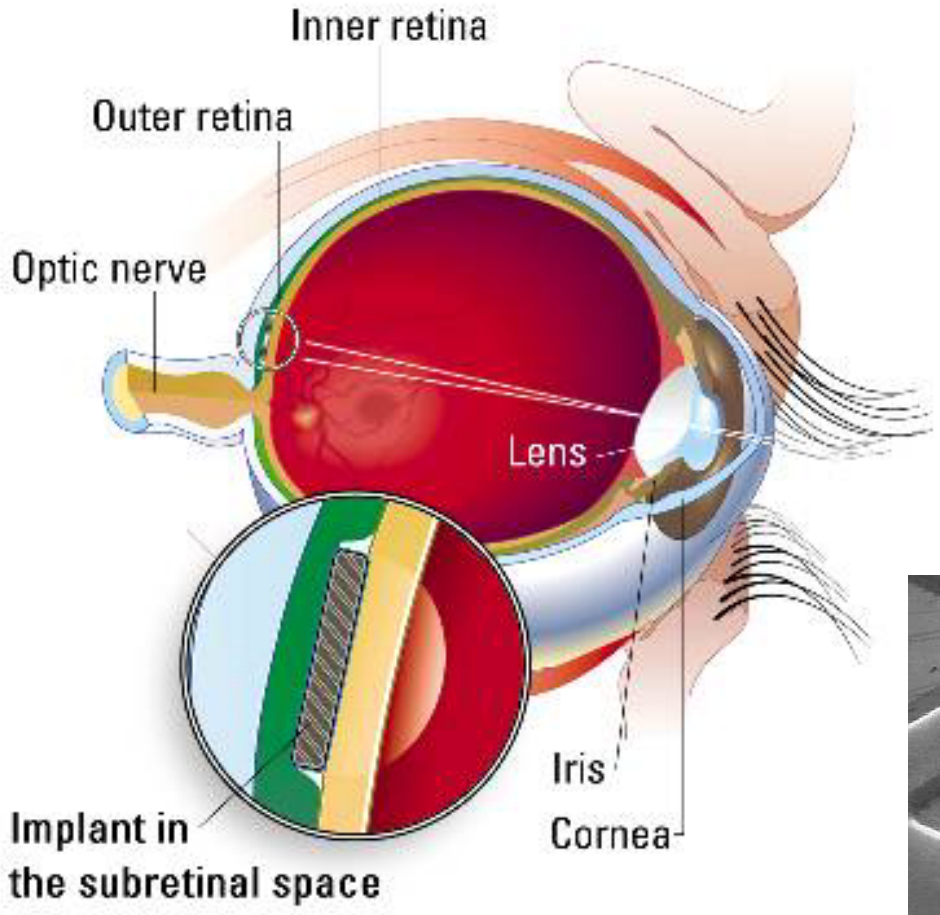
# Linking Si Technology with Biology

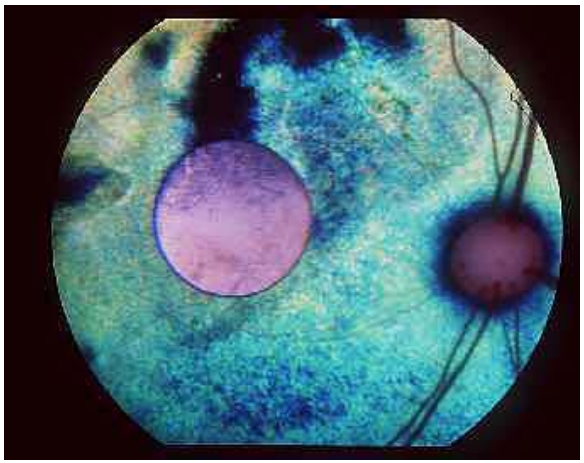


'Snail' neuron grown atop an Infineon Technologies CMOS device that measures the neuron's electrical activity, linking chips and living cells.

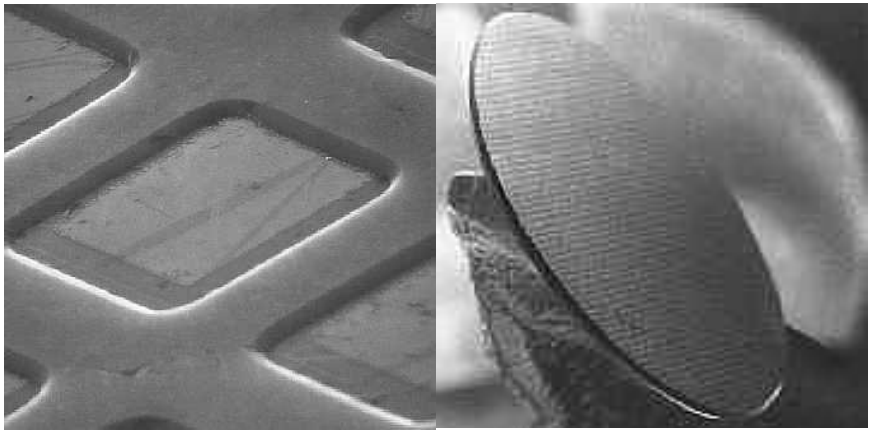
Source: Max Planck Institute

# Artificial Silicon Retina™ (ASR)



2mm, 1/1000” thick



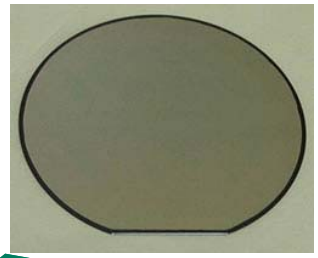
http://www.optobionics.com/index.htm

# Heterogeneous Integration of Microsystems

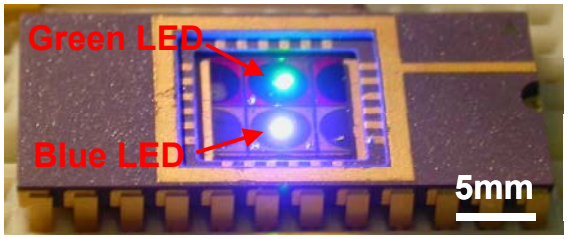
## Professor Nathan Cheung, EECS

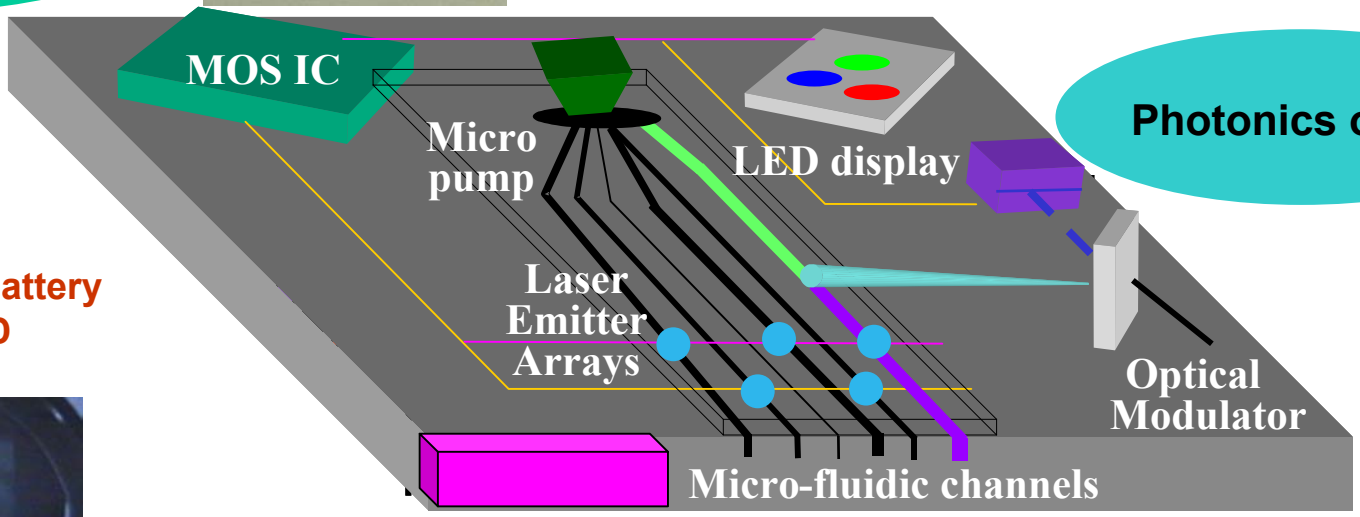
Si-Ge high mobility electronics

GeOI



BioMEMS Emitters /Filter/Detectors

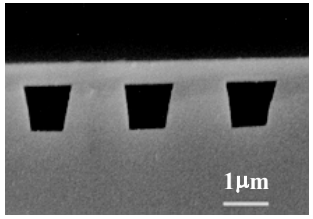



Photonics on Si

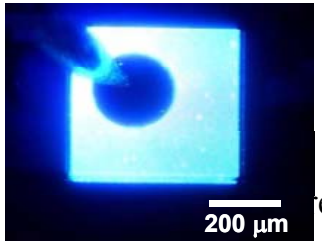
Encapsulated battery with switch/LED

Encapsulated Power source

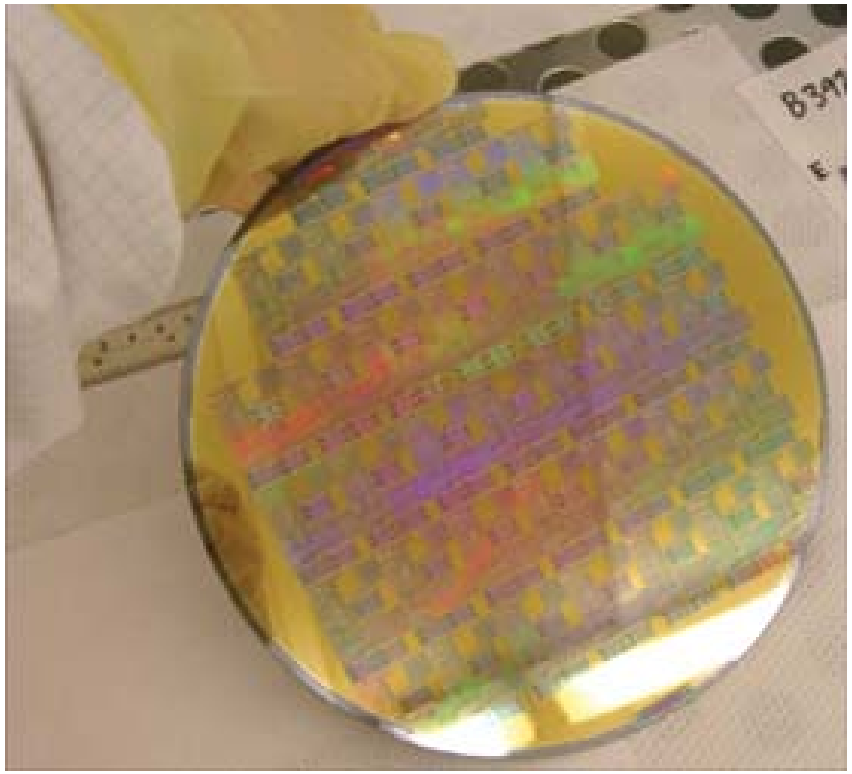



Si microfluidic channels

*InGaN LEDs on Si*

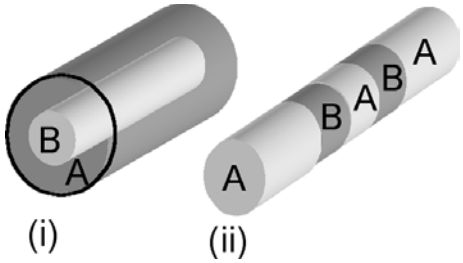


# Extension of Si Technology



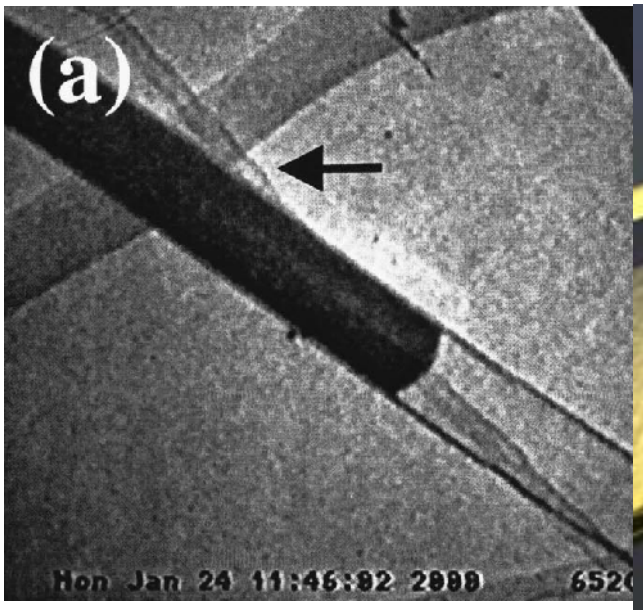
Si circuits on plastic

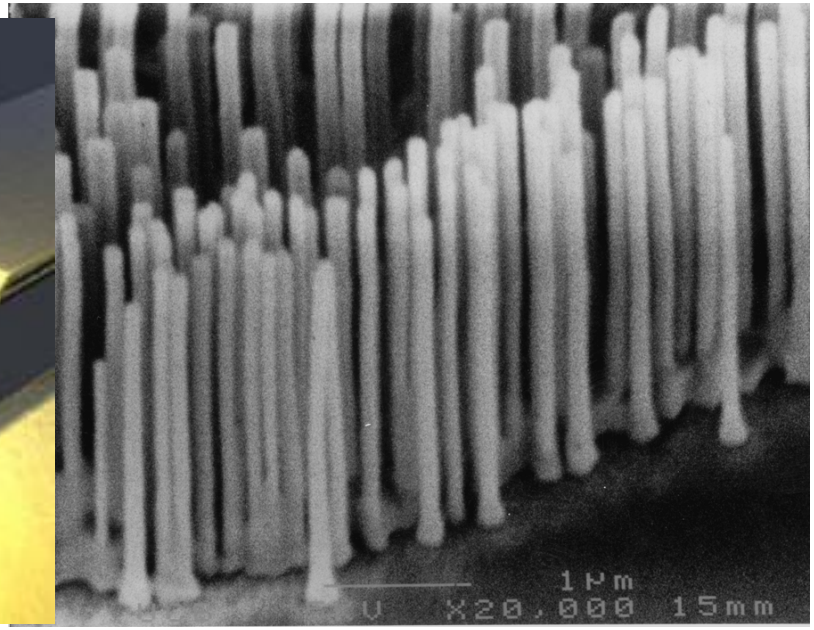
Si Laser (Intel)




# Nanoscale Fabrication

*(i) Co-axial heterostructure nanowire (COHN); (ii) longitudinal heterostructure nanowire (LOHN).*




Carbon Sheath around Ge Core
Peidong Yang, UCB

Carbon Nanotube Motor
A. Zettl, UCB

ZnO nanowire array on sapphire substrate
Peidong Yang, UCB