EECS 143 Microfabrication Technology

Lab Report 1

Table of Contents

1. **Profiles & Layout (14 Points)**
2. **Process Procedures (30 points)**
3. **Calculations (26 Points)**
4. **Questions (30 Points)**
5. **Bonus Questions (10 Points)**

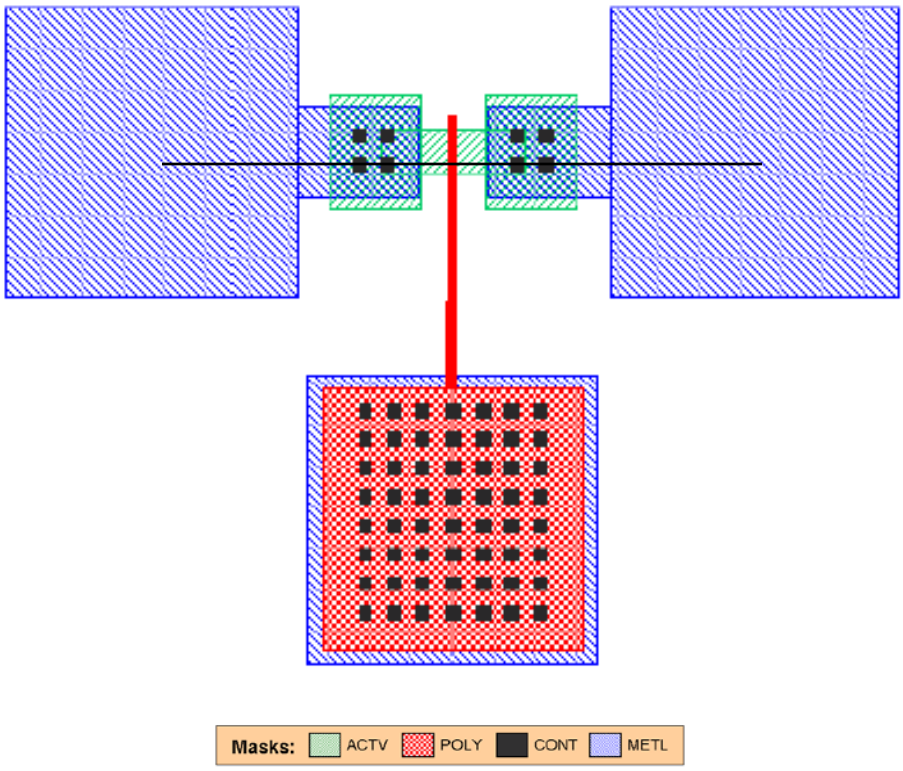
Total Points = 110 possible (graded out of 100)

Please be sure to include the requirement signature regarding academic honesty. All lab group members should print out this page, sign on the attached form, and include it with your Lab Report. Thank you!

Each group of two students will submit one joint report. The report should be organized as follows:

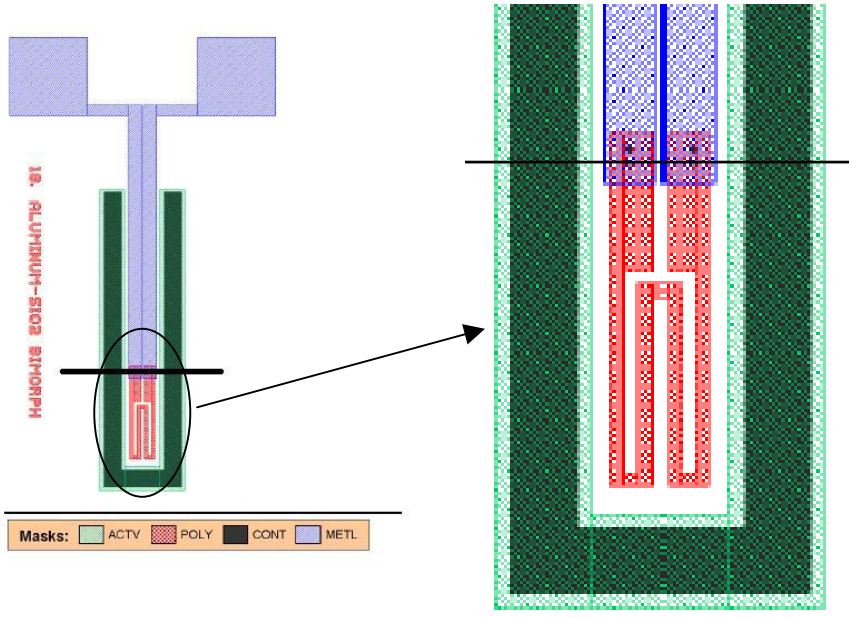
1. **Profiles & Layout (14 Points)**

   A. Draw cross-sectional profiles of a thin-oxide *MOSFET* (test structure 8) after each of the 11 major processing steps. Indicate all layers and specify important details such as the non-planar interfaces, isotropic etch profiles, point-source Al evaporation, thermal oxidation growth, etc. Label each feature and indicate thicknesses (make roughly proportional sketches). These drawings should have significantly more detail than those on the lab manual website. See the diagram below for the exact cross-sections in question. (5 Points)



B. Draw top views of the same thin-oxide *MOSFET* (test structure 8) after each of the four photolithography steps. (4 Points)

C. Draw cross-sectional profiles of the bimorph (*MEMS* - test structure 18) after each of the 12 major processing steps (including XeF_2 release etch), in the same fashion that you did for the MOSFET. See the diagram below for the exact cross-sections in question. (5 Points)



2. **Process Procedures (30 Points)**

   A. List and concisely describe the problems occurred during the fabrication in the class (i.e., nonuniform PR films with some uncovered area, etc.). What were the sources of the problems, and how did you avoid them? Was there any process step that was done somewhat differently from the descriptions in the lab manual? If so, why were some steps done differently and how did it affect the outcome? How do you expect it to affect the performance/function of the device? (10 Points)

   B. Other than the problems that occurred during the session, what were the particular problems (or deviations from the rest of the groups) that occurred in YOUR wafer? What were the causes and how were the problems overcome? Include any pictures/sketches that would be helpful. (10 Points)

   C. Describe monitoring measurements that were done during processing (color, line width, thickness, resistivity, etc.). Determine and describe whether and how much each layer was overetched or underetched? Did you purposely over/underetch? Why? How much each layer was misaligned to the neighboring layers? How much the misalignment acceptable in terms of the device function? You may want to provide pictures taken to determine over/underetch and misalignment. (10 Points)

   We are looking to see that you understand how the process steps work.

3. **Calculations (26 Points)**

   Draw a table with the following parameters from your own wafer: (3 points)

   a) Film thickness (each layer)
   b) Sheet Resistance (after ion implantation and S&D formation)
   c) % over/underetch (each layer)

   Calculate the parameters asked for in the following questions—list both the theoretical values and the empirical values, when applicable. We would like to see that you understand what processing abnormalities may have led to a discrepancy between the two:

   1. Theoretical and empirical thicknesses of field oxide, gate and intermediate oxides (Include orientation dependence of oxidation rate but not impurity dependence) (6 points)
   2. Junction depths after pre-diffusion and drive-in (theoretical, assume only phosphorous doping with surface concentration limited by solid solubility) (5 points)
   3. Final surface concentrations of dopants, as calculated using sheet resistance measurements made in lab. (4 points)
   4. Lateral diffusion under the MOSFET gates (theoretical). (4 points)

5. List an estimate of the Young's modulus, Poisson ratio, and coefficient of thermal expansion for SiO_2, poly-Si, and Al films as deposited. (You can find these in a table in many physics/ME textbooks, or in a web-based search.) (4 points)

4. **Questions (30 Points - 2 points each)**

Answer these questions in the most concise manner possible. A few lines should suffice for each.

1. What type of photoresist (positive or negative? I-line or G-line?) do we use in the lab? Briefly describe how the resist responds to the process steps like spinning, UV light exposure and development.

2. What is the purpose of baking the wafers at 120 °C before depositing HMDS? What is the purpose of the 90 °C bake after spinning on photoresist? What happens if the soft bake is too hot (say 150 °C)?

3. What is the purpose of hard bake? What happens if we skip this step? What may happen if the bake is done at a temperature above 120 °C (say 150 °C)?

4. We do lithography steps under yellow light only. What happens if we expose the wafers to fluorescent light before development? And after development? Would red light damage your process?

5. What are the differences between wet and dry oxidation that lead us to use one for the gate oxide and one for the field oxide? What is the purpose of annealing in nitrogen after gate oxidation?

6. How do you determine etching time theoretically? List two ways to determine etch rate in the lab, when you etch the gate oxide layer in HF. (Hint: the least obvious of these methods includes visual cues.). How close are the experimental and the theoretically calculated values?

7. Before n+ deposition (prior to SOG spinning), we clean in Piranha but not in HF. Before gate oxidation, we clean in both. Why the difference?

8. Why is 5:1 BHF (5:1 NH_4F:HF) used for etching features in the oxide while 10:1 BHF is used for cleaning and p-glass stripping? Why buffered HF?

9. What would happen if we skipped the HF dip before metallization?

10. What is selectivity? What is the selectivity of HF between Si, oxide and PR?

11. Why do we first use the roughing pump and then the diffusion pump when pumping down the aluminum deposition system? Why must the foreline pressure be kept below 100 mTorr?

12. What is the Al etchant composed of? What happens if you use it at room temperature? What is the purpose of sintering? What will result if sintering step is skipped? What happens if sintering temperature is too hot or too low?

13. Briefly explain the mechanism of XeF_2 etching. Is the etch isotropic or anisotropic? Why not use KOH instead of XeF_2?

14. What would happen if a native oxide film was left on the wafers as it went into the XeF_2 etching step?

15. Identify two of the 11 major processing steps that are unnecessary to fabricate a functional oxide cantilever beam. Why are they unnecessary?

5. **Bonus Questions (up to 10 Points)**

   (a) You probably notice that the oxide beams are not rigid mechanically. How will you modify the 143 process flow or layout/structure to achieve a more rigid oxide beam? Show your proposed process flow and new structures and discuss how your design will affect the MOS devices. This is an open-ended question and has no unique answer. (5 points)

   (b) What process steps would be different if you were making a PMOS device instead of NMOS? What additional steps would be involved to make CMOS? (5 points)

Updated on October 25, 2005 by Varadarajan Vidya

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Fall 2005

In signing below, I attest to the fact that I have read and have adhered to the policies and guidelines discussed in the EECS Departmental Policy on Academic Dishonesty, as found at: http://inst.eecs.berkeley.edu/~ee143/fa05/policy.html

Name: _____

Signature: _____

Date:_____

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