EECS 143
Microfabrication
Technology

Undergraduate IC-MEMS Processing Laboratory

Introduction and History

The EECS 143 undergraduate course Processing and Design of Integrated Circuits has been designed to familiarize students with fabrication technology, types of device structures, electrical characterization, modeling of devices, and with the relationships between physical layout and electrical characteristics. The course was first offered in 1972 by Professor D. A. Hodges as a graduate course. It was changed into an undergraduate class the following year and joined with an independent laboratory course (EE134) started several years earlier (1968) by Professors W. G. Oldham and W. Howard. When the two courses were joined, the laboratory section was revised from the fabrication of bipolar devices to PMOS transistors and other test structures (EE147).

In 1980, when the Microfabrication Research Facility was designed, the undergraduate laboratory served as a test site for the modular construction planned for the research lab. As a result, two smaller clean room areas, separated by a service chase, were built into the existing large room and advanced processing equipment was installed. At the same time, a new process was developed and introduced in 1981.

The quarter system allowed only 10 three-hour laboratory sessions to complete the processing and to characterize the devices; thus, a simple, 4-mask aluminum gate NMOS process was designed with spin-on doping for source and drain diffusions and metal definition by lift-off. EECS 143 has been offered every semester since its inception and became a popular course not only for undergraduates, but also for those graduate students who are involved in process technology/integrated circuits design and processing.

When the campus changed from the quarter to the semester system, the number of laboratory sessions increased to 15 and it was possible to carry out a more detailed characterization of the test chip. Advanced test equipment was obtained over the years and by this time, following Berkeley's tradition of constant updating of courses, it was also appropriate to change the process to reflect current industry standards more closely. Thus, both the process and test chip were redesigned, and the new chip was introduced during the Fall semester of 1987, which replaced aluminum gates with self-aligned polysilicon gates. In 1995 the layout was redesigned with more robust devices. And due to the high interest of MEMS devices, the layout has been revised again in 2000. Four MEMS structure have been added to the EE143 mask set: A thermal bimorph actuator, a heat platform, a cantilever, and a campanile. These four are intended to be representative of the types of structures being used by the MEMS community.

Course Description

EECS 143 - Processing and Design of Integrated Circuits is a 4-credit undergraduate course, given every semester, with three hours of lecture and three hours of laboratory per week. The course focuses on

- Principles and mechanisms of Microfabrication,
- Device structure and characterization,
- Relations between physical layout and electrical characteristics,
- Surface-micromachining technology.

MOS transistors and simple circuit elements are fabricated in the laboratory and electrically evaluated. The MEMS structures can be activated with electrical heating. The prerequisite course is EE40 – Introduction to Microelectronic Circuits **OR** EE100 – Electronic Technique to Engineering. For students without Semiconductor Physics/Devices background, EECS 143 will provide a brief introduction to these topics.

Facilities

An independent laboratory with an area of approximately 840 square feet is maintained for EECS 143 in 218 Cory Hall. Maintenance of the processing equipment is provided by Microlab staff, and of the characterization instrumentation by the EECS Electronics Support Group.

The equipment is arranged to provide optimum conditions in which a group of 8 students can operate, each pair processing one wafer. There are essentially three working areas, two of which are maintained under clean room conditions for processing:

1. the photoresist clean room, where resist spinning, baking and alignment are done; aluminum evaporator for metallization, and Nanospec and four-point probe, where thin film thickness and sheet resistance measurement are done;
2. the diffusion and etching clean room with 3 furnaces, and two wet process stations for the rest of the operations;
3. the characterization area with five probe stations for electrical testing with the aid of five HP 4145 Semiconductor Parameter Analyzers and a laserjet printer. There are also six computers with Microsoft Windows 2000 operation system; class accounts are given out at the beginning of the semester. Students are required to perform process simulations using SUPREM. The laboratory's equipment is listed in the attached table.

Test Chip Layout

The test chip was laid out using the KIC graphics editor. Each device was laid out as a separate cell, so that they could be placed as instances once the chip was ready to be "assembled". This facilitated a compact arrangement of devices on the final chip. Devices with repeating structural units, such as the ring oscillator, were also laid out using instances of the basic unit.

Included on the chip were many of the test structures from the original design, along with several new ones. There are four main groups of structures:
1. Resolution test patterns, resistors and capacitors for process characterization (No.'s 1-6);
2. Diode, n-channel MOSFET's and lateral BJT's (No.'s 7-13);
3. Inverter, NOR-gate, ring oscillator, contact resistance for simple circuit measurements (No.'s 14-17);

4. Aluminum-SiO_2 Bimorph, campanile, cantilever array, heater platform as MEMS devices (No.'s 18-21).

Process

The 4 mask NMOS process starts with 3" p-type wafers of 3-5 ohm-cm resistivity, which were blanket-implanted with boron before initial oxidation. This serves as both the field and the device threshold implant, which was moved to the beginning of the process to avoid delays during the semester. After initial oxidation (5000 A) the active (n+ diffusion) area is defined with Mask I (ACTV). This is followed by gate oxidation (800 A) and poly-silicon deposition (3500 A). Mask II (POLY) defines the gate. The poly-Si is wet etched and the active area is BHF dipped clean for n+ diffusion, taking advantage of the self-aligned source/drain feature of poly-Si gates. A spin-on phosphorous-silica film is used as the source for n+ diffusion. After drive and oxidation, Mask III (CONT) is aligned and contact openings are etched with BHF. After aluminum evaporation, Mask IV (METL) is printed and Al is defined by wet etching. Sintering is the final step and the process is completed. For the MEMS device, the process are the same as the 4 mask NMOS process, with the XeF_2 etching as the final step to release the MEMS structures.

Laboratory Operations

Teaching assistants (TA's) for this course are recruited from among those graduate students who are experienced in semiconductor processing and are users of the Microfabrication Facility, the graduate research laboratory on the 4th floor of Cory Hall. This is to ensure that they have the background necessary to independently conduct a processing laboratory. Also, because of safety restrictions, there are no provisions in the EECS 143 lab for doing the polysilicon deposition and XeF_2 etching of silicon. The students go to the Microlab for that session where they can see a modern wafer processing facility and, with the aid of the TA, use the LPCVD furnace to deposit polysilicon on their wafers and XeF_2 to release the MEMS structures.

The maximum number of students that can be accommodated per semester is 64; 8 students/session, with two 3-hour sessions per day with Monday mornings and Friday afternoons left open for maintenance. The head TA conducts one section and takes care of scheduling laboratory preparation, equipment problems, etc. The others handle two sections each. Office hours are held by each TA separately, also in the lab, one hour per week.

Students work in pairs throughout the semester and submit joint lab reports: the first one at the end of processing; the second report after characterization, at the end of the semester.

To allow sufficient time towards the end of the semester for electrical characterization, students are given a mask set and start with oxidized wafers; thus the first step they become familiarized with in the lab is photolithography. All operations are done by students; TA's are there to guide them. During the waiting periods they are assigned to run SUPREM simulations and are allowed to familiarize themselves with the measurement equipment.

Testing equipment is arranged such that there are four five stations available; thus all four pairs in a section can work simultaneously. All five stations are connected to HP4145 Semiconductor Parameter Analyzers, on which the measurements are done. One of the stations is the C-V probe station, which is used to measure the capacitors.

Conclusions

We have introduced a new process and test chip in the laboratory of EECS 143 during the Fall Semester of 1987, further tested it during Spring 1988, redesigned the chip during the Winter of 1994, put the lab manual on-line during the Spring of 1995, and added MEMS structures to the mask in Fall 2000.

The characterization and parameter extraction part which is the most important experience the students receive from the course, had been extended, requirements described in detail and presented in a systematic manner. With this we hope to increase the students' level of understanding of semiconductor and surface machining process engineering, and to enhance the overall value of the course.

Acknowledgements

Our appreciation and thanks go to Professors D. A. Hodges and W. G. Oldham, who envisioned and created this course, and provided the information about the early days; to those graduate student teaching assistants who, over the years, cared enough to suggest improvements both in the laboratory material and in facilities; and to Professor N. Cheung who arranged for the vast improvement of the testing equipment. Credit goes to Matt Mathew, Professor T.J. King and Professor C. Pister for incorporating the present MEMS structures on the chip.

Microlab staff supports the process and processing equipment. The Electronic Support Group maintains the test instrumentation.

K. Voros, Spring, 1994
Updated by C. Sun, Fall, 2001