Homework Assignment # 11 (Due Dec 1) [11/24 is Thanksgiving Holiday]

Required Reading

(1) Visit the Device Visualization website http://jas.eng.buffalo.edu/
(a) Run all four simulation of the MOS capacitors (set Q_{ox} =0 first and then see effect of Q_{ox})
(b) Run all three MOSFET simulations on http://jas.eng.buffalo.edu/
Start with http://jas.eng.buffalo.edu/education/mos/mosfet/mos_0.html
(2) EE143 Reader Week #10 assignment on MOS field effect transistor. If you need more details on MOS devices, visit http://inst.eecs.berkeley.edu/~ee130/

Problem 1 Simple threshold voltage calculation

An NMOS transistor has V_{TN} = +0.7 volts when the p-substrate concentration is $2 \times 10^{16} cm^{-3}$. n+ poly-Si is used as the gate material. What is the gate oxide thickness ? Assume there is no body bias and no oxide charges.

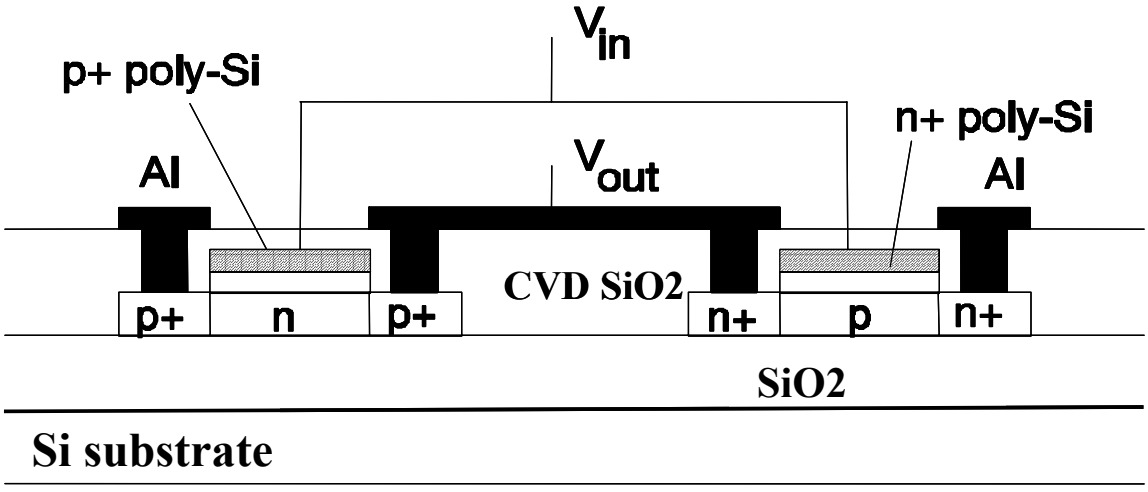
Problem 2 Given V_T and Q_f, find range of substrate doping

For n^+ poly-gate NMOS, the design goal is to make V_T to be within the range of 1.0 ± 0.3 volts. The gate oxide thickness is 0.1 μm and both V_S and V_B=0. Find the range of substrate doping concentration which will lie within the V_T tolerance for the following two Si substrate orientations: (i) (100) with $Q_f/q = 10^{10}$ / cm^2 (ii) (111) with $Q_f/q = 5 \times 10^{10}$ / cm^2

[Hint: The solutions for doping concentration can be obtained by using numerical iteration]

Problem 3 CMOS threshold voltage calculations

The following figure shows the cross-section of a CMOS inverter made with Silicon-on -insulator (SOI) wafers.



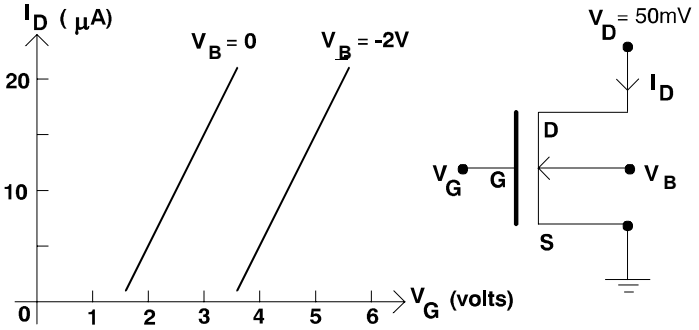
(a) For the CMOS transistors, the gate oxides are 0.05 μm and oxide and interface charges are assumed to be zero. p^+poly-gate is used for the p-channel device and n^+ poly-gate is used for the n-channel device. If we would like to have V_T (n-channel) = +1volt and V_T (p-channel) =-1V, calculate the required channel doping concentrations for both devices.

(b) Keeping the same channel doping concentration for the PMOS but replacing the gate with n+ poly-Si. What will be the new threshold voltage?

(c) Suppose we would like to restore the threshold voltage of the PMOS described in part (b) to –1V again by performing a threshold tailoring implantation step in the process flow. What doping specie will you choose? What will be the required dose?

Problem 4 Simple MOSFET I-V Analysis

The I_D versus V_G curves for a n-channel enhancement-mode MOSFET with a fixed V_{DS} (=50 mV) are shown below. The transistor channel length is 10 μm and the channel width is 100 μm, with a gate oxide thickness of 1000 Å.

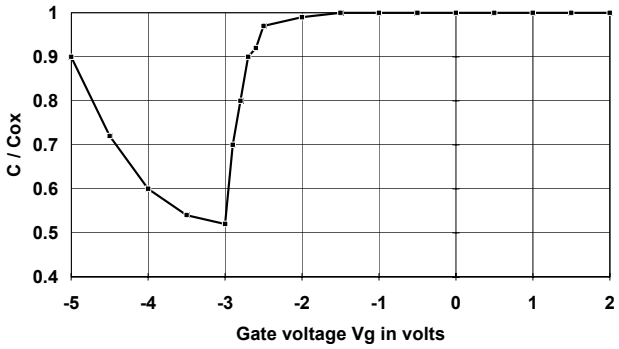


(a) Find the threshold voltages for (i) V_B=0 and (ii) V_B=-2V.
(b) Find the substrate doping concentration (assume the substrate is uniformly doped).
(c) Find the carrier mobility in the channel.
(d) Find I_{Dsat} of the transistor for V_B=0 and V_G =10V .

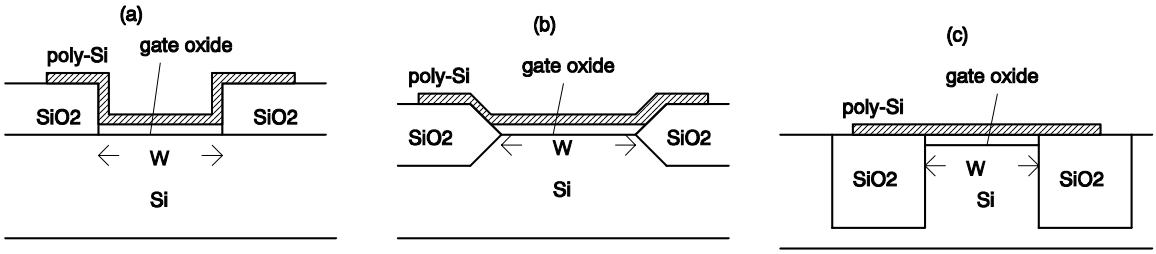
Problem 5 C-V Analysis

Experimental MOS data of C / C_{ox} versus V_G are given below . It is known that the oxide thickness is 0.26μm, the SiO_2-Si interface charge Q_f= +3.6× 10^{11}q /cm^2.

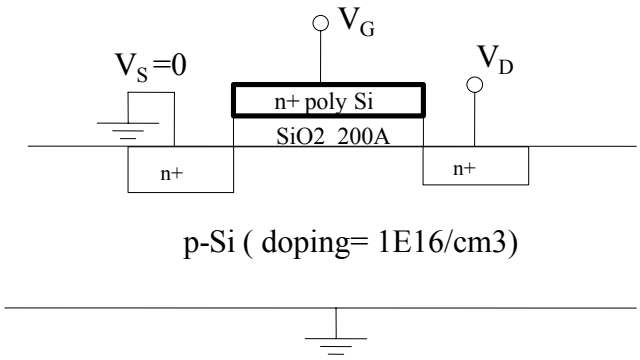
(a)Calculate the maximum depletion layer thickness, x_{dmax}
(b)Estimate the substrate doping concentration N_a (ANSWER REQUIRES ITERATION)
(c) Calculate the work function of the gate material.



Problem 6 MOS Narrow Width Effect
For identical **channel widths** W, discuss which one of the following three oxide isolation schemes will exhibit the most narrow width effect.: (a) oxide window, (b) LOCOS and (c) trench oxide isolation. Illustrate your answer with sketches or a few sentences. [Note: the cross-sections are along the channel width direction, NOT the channel length direction]


(a)
poly-Si
gate oxide
SiO2
SiO2
W
Si
(b)
poly-Si
gate oxide
SiO2
SiO2
W
Si
(c)
gate oxide
poly-Si
SiO2
W
SiO2
Si

Problem 7 Past exam question



The following cross-section shows a NMOS transistor with **n+ poly-Si gate**, gate oxide thickness = 200 Å, and a p-substrate with doping concentration = 1E16/cm^3.

(a) Thermal SiO2 will have electrical breakdown when the electric field is > 8×10^6 V/cm. What is the **maximum** V_G that can be applied without causing gate oxide breakdown?

(b) If there is no oxide or oxide interface charge, calculate the threshold voltage V_T for V_D =0.

(c) Calculate the thickness of the depletion region (x_{dmax}) underneath the gate oxide when V_G= V_T , with V_D =0.

(d) Calculate the drain current for V_G = V_D = 5 volts. Use k =50 μA / V^2.

Note: I_{DS} (triode region) = k [(V_G- V_T) V_{DS} - V_{DS}^2 /2] ; I_{DS} (saturation region)=k[(V_G-V_T)^2/2]

(e) If a boron threshold implant is performed with a dose of 10^{12}/cm^2. What is the new threshold voltage of the transisitor.[You can assume the boron implant concentration profile is a delta function located exactly at the Si/SiO2 interface].

(f) What is the drain current for V_G = V_D = 5 volts for the MOSFET with the boron threshold implant described in part (e)?

(g) A small-signal C-V measurement across the gate and substrate terminals is performed with the MOSFET structure. V_D is grounded to zero voltage. Sketch qualitatively the C versus V_G curve from –10V to +10V.

(h) Calculate the maximum C value (in F/cm^2) and the minimum C value (in F/cm^2).