Homework Assignment # 8 (Due Nov 3, Thur 9:30am)

Reading Assignment

Introduction: Chapter 7 of Jaeger on Interconnect and contacts
Brief description of CMP Section 3.8.2 of Jaeger.
EE143 Reader,Chapter 15 Campbell on metallization [You can skip sections 15.1 and 15.5]

Problem 1 Simple resistance and capacitance calculations

Aluminum-copper-silicon alloy as an interconnect material has a resistivity of 3.2 μohm-cm.
(a) What is the sheet resistance of a 1-μm-thick film.
(b) What would be the resistance of a line 500 μm long and 10 μm wide?
(c) What is the capacitance of this line to the substrate if it is on an oxide (SiO2) which is 1 μm thick? You can assume the substrate is heavily doped so that you can use the parallel-plate capacitance formula.
(d) What is the RC time constant associated with this 500 μm-long line?
(e) If the oxide is replace by a new low-K dielectric (relatively permittivity =2), what is the new RC time constant ?

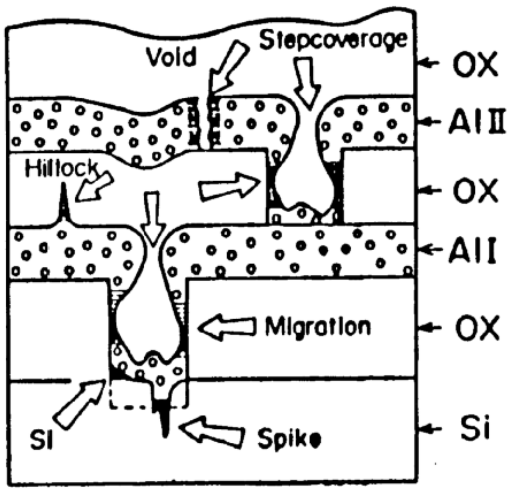
Problem 2 Electromigration failure

a) Electromigration failure time depend exponentially on (1/temperature).
What is the ratio of the MTFs of identical aluminum interconnects operating at the same current density at 300 K and 400 K? Use an activation energy E_A = 0.5 eV for electromigration failure.

b) For interconnect reliability, design rules are used to ensure the current density is below a certain value. What is the maximum current that may be allowed to flow in an aluminum conductor 1 μm thick and 1 μm wide if the current density must not exceed 5 x 10^5 A/cm^2

Problem 3 Issues with Al metallization

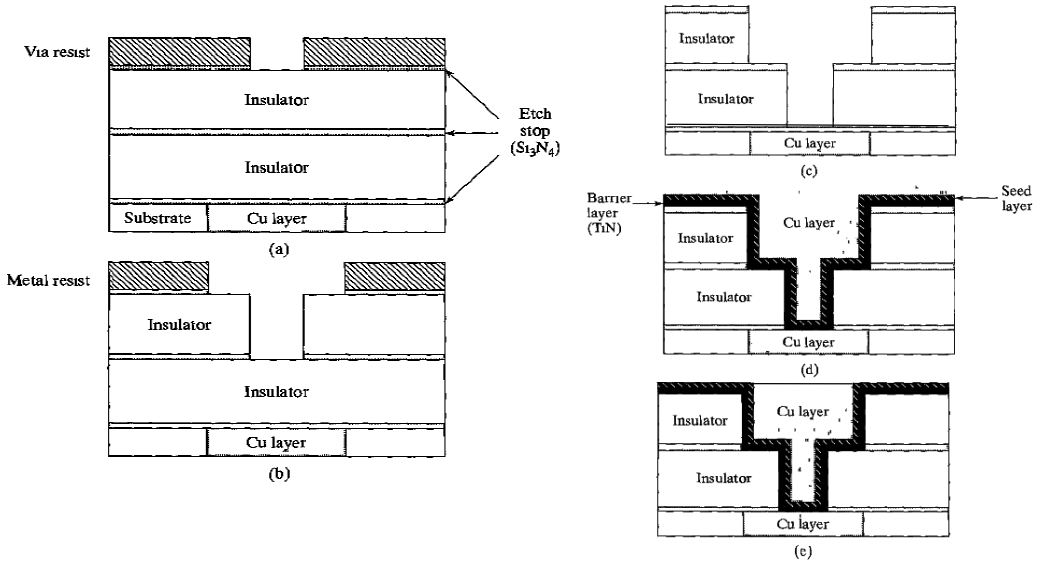
The following cartoon shows some major problems of using Al as the metal for multilevel metallization. Describe your understanding of the origins AND methodologies used to minimize/eliminate such problems.



(a) Hillock and Void formation in interconnects
(b) Al spiking into silicon substrate. [In particular, why the spikes are deeper if they occur near perimeter of the contact holes?]
(c) Step coverage problem

Problem 4 Damascene Process

Your textbook [Jaeger, Chap 7] shows the following process sequence to fabricate a metallization system using Copper as the metal (The Dual Damascene Process). Some steps are skipped in the sequence of cartoons drawn. Make sure you understand the complete sequence flow.



(i) Cu is used to implement **TWO** metallization structures in this process. Name these TWO mtallization structures.

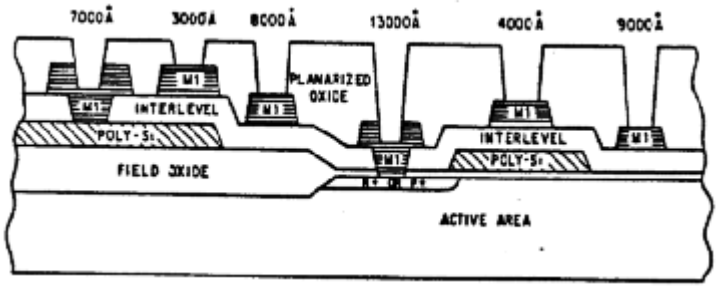
(ii) The "Seed layer" is a very thin layer of TiN , deposited by CVD. What are the **TWO** major functions of the TiN layer ?

(iii) The Chemical-Mechanical Polishing (CMP) step is used once in the process flow. Which step is it?

(iv) If the Si3N4 etch stop layers are omitted, what will be the problem(s) ? Illustrate with a sketch.

Problem 5 Planarization

The following cross-section (Fig.A) shows a poorly planned planarization process with planarization starting only at the Planarized Oxide step.



(a) What difficulties you will encounter when etching contact holes through the Planarized Oxide to reach the Metal-1 (M1) surface ?

(b) Instead of using LOCOS to form the Field Oxide, propose another isolation oxide structure to achieve better planarization. Sketch Fig.A again with your proposed isolation.

(c) Continue with your structure in part(b), let us improve the planarization by performing a planarization step after the interlevel dielectric layer is deposited. Sketch Fig.A again.

(d) After part(c) , you find you can still improve the planarization by putting a tungsten plug between M1 and the substrate N+ or P+ contact. Sketch Fig.A again with this improvement.