Homework Assignment #1 (Due September 15, 9:40am in class)

Required Reading

1)"Introduction to Microengineering" by Danny Bank in EE143 Reader
2) Streetman, Chap 3, "Energy bands and charge carriers in semiconductors" in EE143 Reader [We will focus on dopant effects, carrier concentrations, carrier mobility , and resistivity for now. You can ignore the E-k diagrams and Hall Effect sections. We will come back and revisit Fermi levels, energy levels, and built-in potentials in later weeks]
3) Chapter 1 of Jaeger
4) Lecture Notes 1,2 ,3 ,4
5) Overview of pn diode process flow
http://jas2.eng.buffalo.edu/applets/education/fab/pn/diodeframe.html

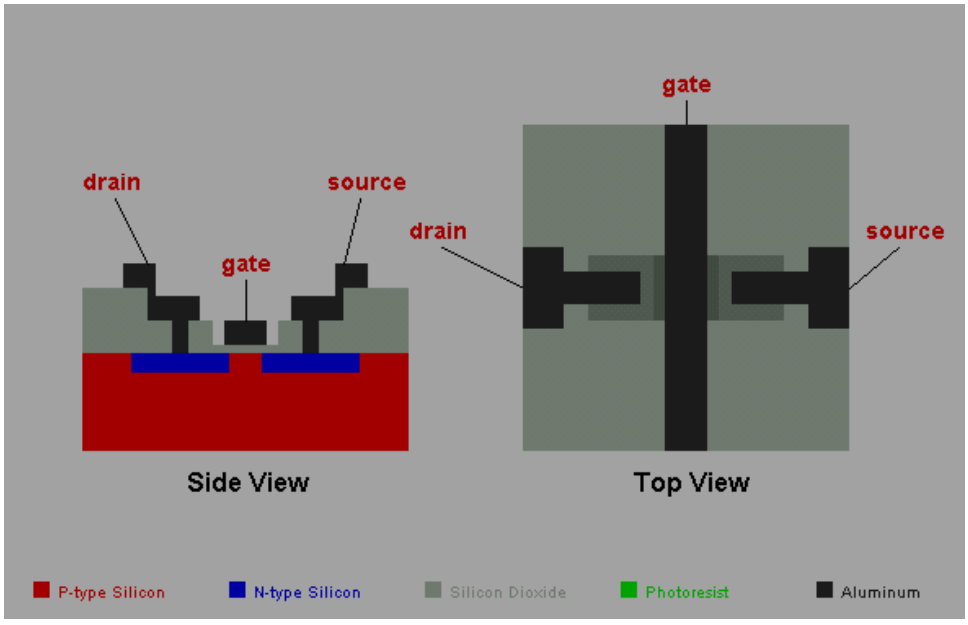
Problem 1 Processing Module Terminologies

(a) Growing an oxide is not the same as Depositing an oxide.
(i) What processing step is used to "Grow" an oxide on a Si wafer ?
(ii) What processing step is used to "Deposit" an oxide on a Si wafer ?
(iii) Discuss briefly the Si substrate consumption between the two processes.

(b) The term "mask" is used with different context in microfabrication literature. Explain briefly:
(i) What is a photomask?
(ii) What is an etching mask ? Quote one example.
(iii) What is an oxidation mask? Quote one example.
(iv) What is an implantation mask? Quote one example.

Problem 2 Process Flow of a simple MOSFET

Visit the website http://jas2.eng.buffalo.edu/applets/education/fab/NMOS/nmos.html which shows the process sequence of a MOSFET using aluminum as the gate material. See the side view (cross-section) and top-view below.

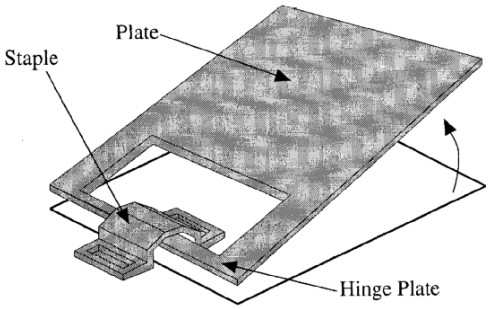


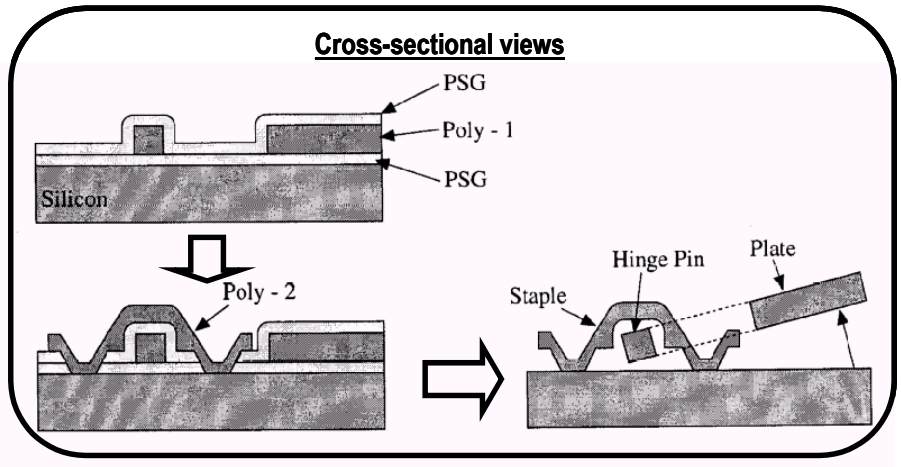
Answer the following questions

1) How many lithography steps are used in this process flow? Discuss briefly the purpose of each lithography step.
2) Why the photoresist has be stripped before the two-step diffusion process which is used to form the source and drain regions?

Problem 3 Processing Steps and Simple Process Sequence

In class, we discussed a simple process flow to fabricate a hinge plate which can create an out-of-plane motion.





(i) Starting with a blanket Si wafer, how many photolithography steps are used to fabricate this device. For each lithography step used, briefly describe its purpose.

(ii) How many chemical vapor deposition (CVD) steps are used to fabricate this device. For each CVD step used, briefly describe its purpose.

(iii) How many thin-film etching steps are used to fabricate this device. For each etching step used, briefly describe its purpose.

(iv) Can one form the staple structure **BEFORE** forming the hinge plate structure in the process sequence ? Explain why or why not .

(v)Your classmate suggests that poly-2 can be replaced by aluminum as the staple material. Do you agree or disagree with this suggestion? Justify your answer.

(vi) Instead of using PSG as the sacrificial layer between poly-1 and poly-2, one can form a thermal oxide by oxidizing poly-1. **Sketch the cross-section of the final structure** after sacrificial layer removal. **Highlight/label the differences** between this cross-section and the one shown in the above figure.

Problem 4 Carrier Concentrations and resistivity

A Si crystal is homogeneously doped with phosphorus to a concentration of $2 \times 10^{17}/cm^3$. By mistake, a second impurity --either boron or arsenic (but not both) is added during the process sequence. The resultant hole concentration is determined to be $2 \times 10^{17}/cm^3$.

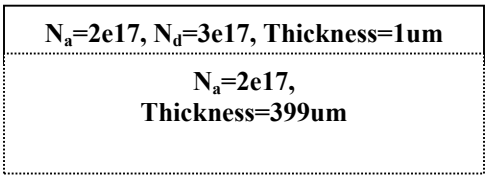
(a) Is the Si p-type or n-type after adding the second impurity?
What is the **minority** carrier concentration?

(b) Is the second impurity boron or arsenic?
What is the concentration added mistakenly?

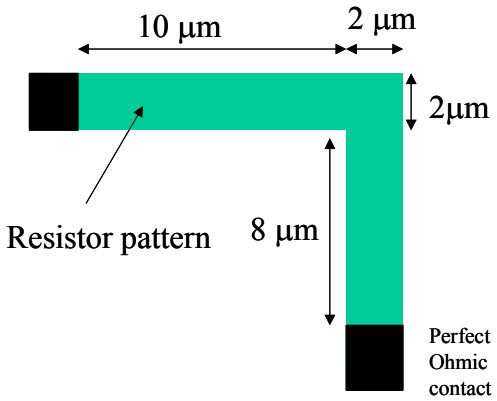
(c) The crystal is then doped further with the addition of arsenic (arsenic concentration = $10^{18}/cm^3$). Find the resultant electrical resistivity.

Problem 5 Sheet Resistance

A Si wafer has a total thickness of 400 μm, with boron concentration of $N_a = 2x10^{17}/cm^3$. The top 1 μm is then uniformly doped with by arsenic ($N_d = 3x10^{17}/cm^3$).



(a) Calculate the sheet resistance R_S of the Arsenic doped layer. .Ignore the depletion width in calculation. Do holes in the bottom bulk of the wafer contribute to the measured sheet resistance? Explain your answer.
(b) A resistor layout pattern is laid out shown in the sketch below (**shown is top view of resistor pattern**). Find the resistance of this IC resistor.



To get Electron and Holes Mobility Curves (for Problems 4 and 5), a large pdf picture can be downloaded in Lec-3 Notes from course website.