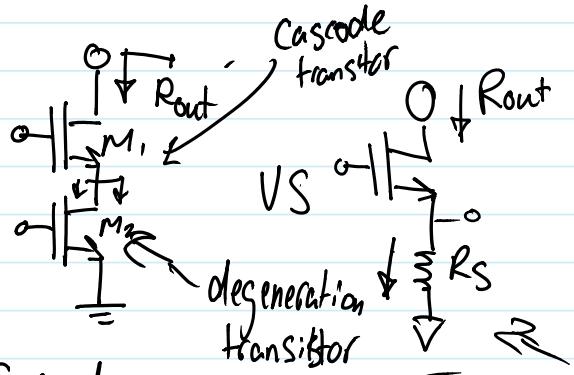
Discussion 4

Wednesday, February 20, 2013 3:10 PM

MOS Cascode



Area, Resistor are hard to define on chip

Want high R_o

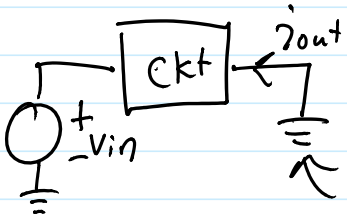
$R_S \cdot I_O$ might be too big

$$R_{out} = (1 + g_{m1} r_{o2}) r_{o1} \simeq g_{m1} r_{o2} r_{o1}$$

typically large

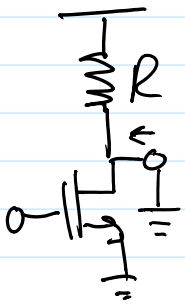
Cascode as amplifier

"Short ckt" trans conductance



$$G_m = \left.\frac{i_{out}}{v_{in}}\right|_{v_{out}=0}$$

output is shorted to Ac gnd



$$A_v = -g_m R$$

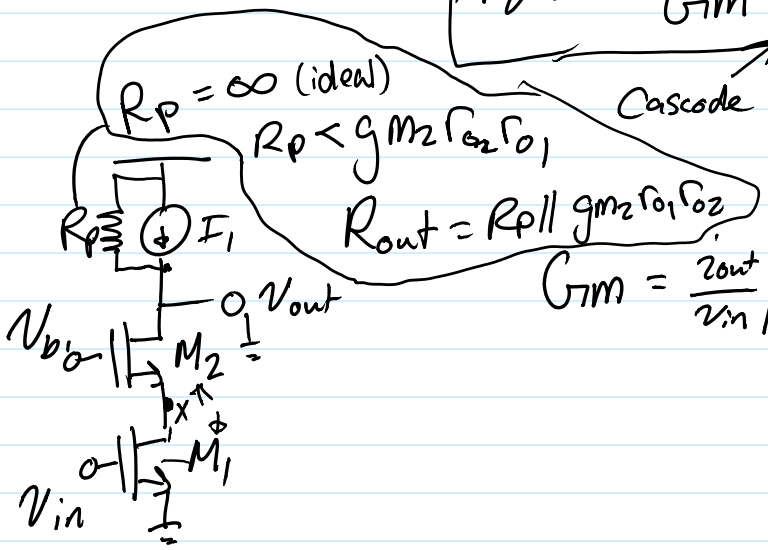
g_m

$G_m = g_m$

Voltage gain of linear ckt

$$A_v = -G_m \cdot R_{out}$$

Cascode output R when input is shorted



$$G_m = \frac{i_{out}}{v_{in}}\Big|_{v_{out}=0} = \frac{v_x}{v_{in}} \cdot \frac{i_{out}}{v_x}$$

$g_{m1} \cdot \frac{1}{g_{m2}} \| r_{o1}$ $\quad$ g_{m2}

$\frac{1}{g_{m2}} \ll r_{o1}$

$$G_m = g_{m1} \cdot \frac{g_{m2}}{g_{m2}} \approx g_{m1}$$

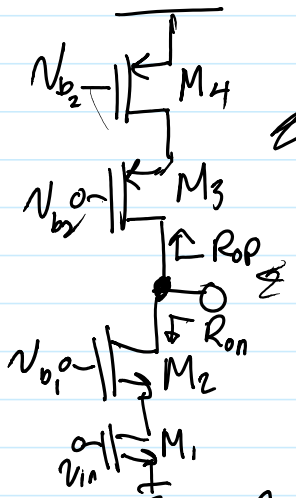
earlier

$A_v = -G_m R_{out}$

$(g_{m2} + g_{mb2})$

$A_v = -g_{m1}(g_{m2} r_{o2} r_{o1})$ gain is boosted $g_{m2} r_{o2}$

$(W/L)_1$ does not have to $= (W/L)_2$



needed to maintain large gain

$R_{on} = g_{m2} r_{o2} r_{o1}$

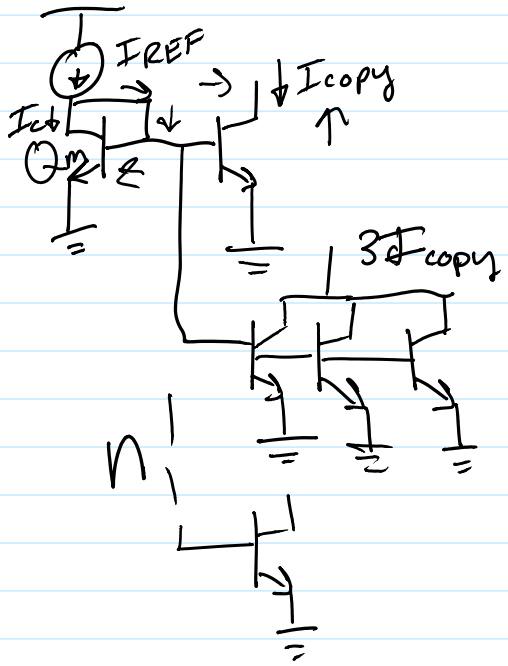
$R_{op} = g_{m3} r_{o3} r_{o1}$

$G_m = g_{m1}$ $\quad$ $R_{out} = R_{op} \| R_{on}$

$\tau_{out} = R_{out} \cdot C_{out}$

$$A_V = g_{m1}[(g_{m2} r_{o2} r_{o1}) \| (g_{m3} r_{o3} r_{o4})]$$

Current Mirrors



Ideal

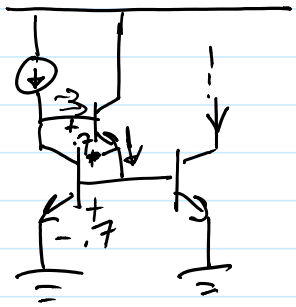
$$I_{copy} = I_{REF}$$

$$I_{REF} = I_{copy} - \frac{(n+1) I_{copy}}{\beta}$$

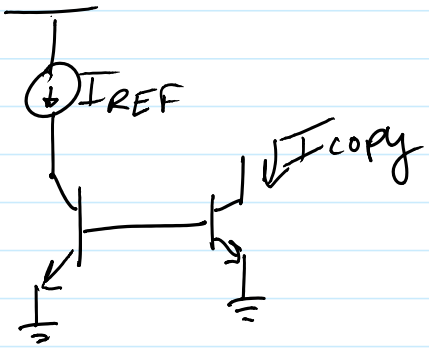
$$I_{copy} = \frac{I_{REF}}{1 + \frac{n+1}{\beta}}$$

if $(n+1)$ is large the currents will not match

β helper design



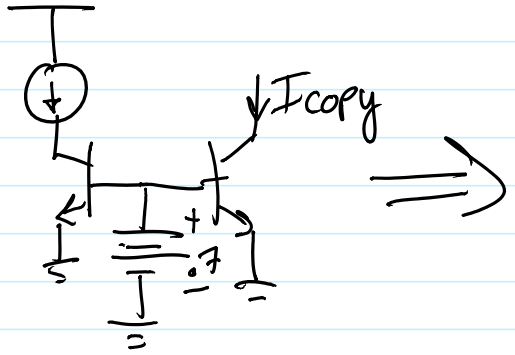
$$I_{copy} = \frac{I_{REF}}{1 + \frac{1}{\beta^2}(n+1)}$$

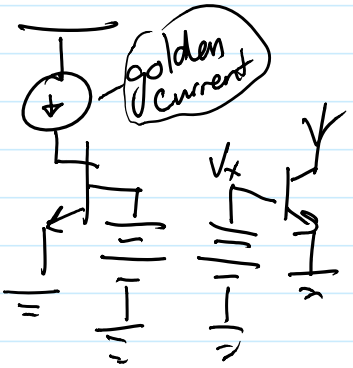


$$\frac{I_{REF}}{1 + \frac{1}{\beta}}, \quad 0$$

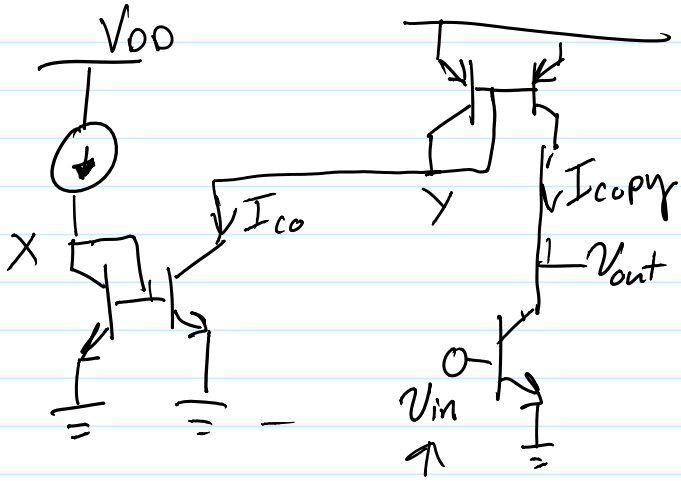
$I_{copy} = 0$ because No path for base currents

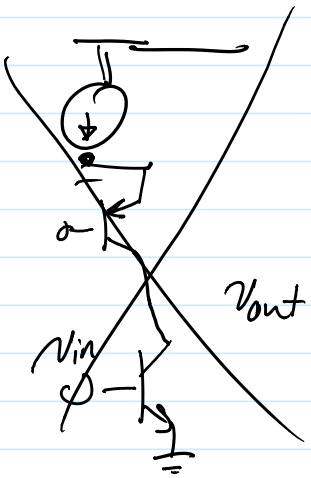
$I_{copy} = 0$ because No path for base currents V_{be} is not defined





$$I_{copy} = I_S e^{V_x/V_t}$$





P3 $\lambda = 0$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$