Modelling the Bipolar Junction Transistor (BJT)

Physically, BJTs are just back-to-back pn junctions

\[ \text{n-p-n bipolar transistor} \]
\[ \text{p-n-p bipolar transistor} \]

Regions of Bipolar Transistor Operation

<table>
<thead>
<tr>
<th>EBJ</th>
<th>CBJ</th>
<th>Mode</th>
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</thead>
<tbody>
<tr>
<td>R</td>
<td>R</td>
<td>Cut-off (both diodes off)</td>
</tr>
<tr>
<td>F</td>
<td>R</td>
<td>Forward Active (widely used in analog amplification, etc.)</td>
</tr>
<tr>
<td>R</td>
<td>F</td>
<td>Reverse Active</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>Saturation</td>
</tr>
</tbody>
</table>

⇒ can also think of this in a convenient graphical sense:

Reverse Active

\[ V_{be} (V_{bc}) \]

Forward Active

Cut-off

\[ V_{be} \]

1. Cut-off Region - (n-p-n transistor)

⇒ both diodes reverse-biased

⇒ no current flows:

\[ I_e = 0, I_c = 0, I_b = 0 \]
Forward-Active Region - (npn Transistor)

- BJE Forward-Biased (i.e., diode on), BJT Reverse-Biased (i.e., diode off)

Forward biasing of the BJE generates three current components:

1. $e^-$s injected from emitter to base: $I_{EB} = -A J_{EB}^{diff}$
2. $h^+$s injected from base to emitter: $I_{BE} = A J_{BE}^{diff}$
3. Recombination of $e^-$s + $h^+$s in base: $I_{RE}$

$$I_C = I_{EB} + I_{BE} + I_{RE} = 1 + 2 + 3$$

$$I_{EB} = -A J_{EB}^{diff} = -AD_{EB} e^{\frac{V_{BE}}{V_T}}$$

$$I_{BE} = A J_{BE}^{diff} = AD_{BE} e^{\frac{-V_{BE}}{V_T}}$$

$$I_{RE} = \frac{[P_{ef}(0) - P_{ef}(-W_B)]}{W_B} = \frac{P_{ef}(0)}{N_{ef}} $$

$$P_{ef}(0) = N_{ef} e^{\frac{V_{BE}}{V_T}}$$

$$P_{ef}(-W_B) = 0$$

Could also replace by diffusion length, $L_D$ (for $L_D$ in $\mu m$ leads)
Define Forward Current Gain $\beta_F$:

$$\beta_F = \frac{I_C}{I_B} = \frac{\frac{qA_D}{N_e N_{eB} V_T} \cdot \frac{N_{eB}}{N_e} \cdot \frac{1}{\frac{1}{N_{eB}} + \frac{g_{mD}}{N_e N_{eB} V_T^2}}}{\frac{g_{mD}}{N_e N_{eB} V_T} + \frac{1}{2} \cdot \frac{N_{eB}}{N_e} \cdot \frac{1}{\frac{1}{N_{eB}} + \frac{g_{mD}}{N_e N_{eB} V_T^2}} - 1}$$

To maximize $\beta_F$, want:

1. $W_B$ is small
2. $N_{eB} \gg N_{eB}$ (this is why emitter is n+)
3. $T_B$ large

More Complete Expression for $\beta_F$:

$$\beta_F = \frac{N_{eB} W_B \cdot \frac{D_{eB}}{N_{eB} L_B}}{2 \cdot D_{eB} C_B} + \frac{1}{2} \cdot \left( \frac{W_B}{L_B} \right)^2 + \frac{5}{2} \cdot \left( \frac{D_{eB}}{N_{eB} L_B} \right) + \frac{W_B}{2} \cdot N_{eB} \cdot W_B \cdot \frac{V_T}{2}$$

Where:

- $S_\text{Re}$: Surface recombination velocity
- $D_{eB}$: Diffusion constant
- $N_i$: Intrinsic carrier concentration
- $N_{eB}$: Carrier concentration
- $A_{eB}$: Total emitter area
- $A_s$: Sidewall emitter area
- $\tau$: Minority carrier lifetime
- $L_i$: Diffusion length ($L_i = \sqrt{D_i \tau}$)
- $W_B$: Active base width

**Diagram**

- p+ region
- n+ region
- p-Si
- active area
- surface recombination occurring here
Forward-Active LS Models

So $\beta$ relates $I_b + I_e$. To relate $I_e + I_c$, use KCL:

$$I_b + I_c = I_e + I_c + \frac{I_c}{\beta} = \left(1 + \frac{1}{\beta}\right)I_c$$

$$\Rightarrow I_c = \left(1 + \frac{1}{\beta}\right)I_e = \left(\frac{\beta + 1}{\beta}\right)I_e = \alpha I_e,$$ where $\alpha = \frac{1}{1 + \beta}$

Thus $\beta = \frac{\alpha}{1 - \alpha}$

**Equivalent Large Signal Ckt. Models for Forward-Active BJT**

There are several of these. The most useful are:

- Common Base (CCB)
- Common Emitter (CCE)

But usually, one doesn't have to use these complicated models. Rather, the following usually suffices:

**3 Reverse-Active Region**

= very similar to forward-active region except now:

- BJE reverse-biased
- BCT forward-biased

= one important difference:

$$\beta_R \propto \frac{N_c e^{Q_R}}{N_a e^{Q_R}} \Rightarrow \frac{N_c}{N_a} \ll \frac{Q_R}{Q_e}$$

$since$ collector is $n-$

$\Rightarrow \beta_R$ is much smaller than $\beta_C$

$\Rightarrow$ poor device performance
BJT Saturation LS Models

4. Saturation Region:

- BJT forward-biased $\Rightarrow V_{BC(sat)} \approx 0.8V$ (higher than 0.7V in saturation)
- BJT forward-biased $\Rightarrow V_{BE(sat)} \approx 0.6V$

Result:

$$V_{bc} \Rightarrow \frac{V_{bc(sat)} = 0.6V}{-} \quad V_{be(sat)} = 0.8V \quad V_{ec(sat)} = 0.2V$$

- Current now determined by the attached elements & KCL:
  - $I_e = I_b + I_C$; no longer have $I_b = \frac{I_C}{\beta}$ or $I_C = \alpha I_e$
  - These no longer apply when BJT is in saturation.

When determining IC operating point:

1. Assume forward-active $\Rightarrow$ check in cutoff (rough Vbe?)
2. Determine Vbe.
3. If Vbe = Vbc(sat) = 0.2V, then ok (i.e., it's forward-active); otherwise, must do the
   analysis even assuming saturation.

IV Characteristics of Bipolar Junction Transistor

- $I_C = \alpha I_B$ (a diode-like characteristic)
- $V_{be}$ is the voltage drop across the base-emitter junction.
- $I_C = \alpha I_B$ (approximately)

---

- Really most interested in $I_C = f(I_B, V_{be})$:
  - $I_C = \frac{V_{be}}{V_T} I_B$ (where $V_T$ is the thermal voltage)

- $I_C$ given more accurately by:
  - $I_C = [I_s \exp(\frac{V_{be}}{V_T})] + \frac{V_{be}}{V_T}$
What is happening physically?

1. \( \text{Cex: } V_{ce} \rightarrow x_1 \rightarrow I_{ce} \rightarrow \text{slope of the current line} \)

2. \( \text{Nar: increase } V_{ce} \rightarrow V_{ce} \uparrow \rightarrow x_2 \rightarrow I_{ex} \rightarrow \text{slope of this line} \)

\( \therefore I_{ex} > I_{ce} \)

Thus, \( V_{ce} \uparrow \rightarrow I_{ce} \uparrow \) due to \( \text{reduction} \)

Result: \( I_{ce} = f(I_{b}, V_{ce}) \) in forward-active!

\[ I_{ce} = \frac{I_{b} \exp\left(\frac{V_{be}}{V_{T}}\right)}{1 + \frac{V_{be}}{V_{T}}} \]

This, then, is a more accurate \( I_{ce} \) equation.

**Small-Signal Model in Forward-Active Bipolar Transistors**

**Y-Parameter Model**

If only interested in the forward direction:

\( Y_{11} = 0 \) \( V_{ce} = 0 \)

\( Y_{22} = \frac{2}{\lambda_{21}} \)

\( Y_{21} = \frac{\lambda_{21}}{\lambda_{22}} \)

**Hybrid-\( T \) Model**

Specified by the knee point.
BJT Small-Signal Model

Determine the S.S. elements:

\[
I_c = \frac{1}{\beta} + \frac{1}{\beta} e^{v_{be}/V_T}
\]

\[
g_m \approx \frac{I_c}{V_{be}} \approx \frac{V_{be}}{I_c}
\]

\[
r_e \approx \frac{V_{be}}{I_c}
\]

\[
r_o \approx \frac{V_{be}}{I_c}
\]

... and thus we have the Hybrid-T model:

\[
B = \frac{g_m}{r_o}
\]

\[
r_e \approx \frac{R_o + R_i}{R_o} \approx \frac{1}{r_o}
\]

\[
r_o \approx \frac{V_{be}}{I_c}
\]

**Remarks:**

1. \(g_m\) is independent of device specifics; depends only on temperature (through \(V_T\)) and biasing \(I_c\).
2. Small-signal model valid for \(V_{be} < V_T \approx 26\text{mV} @ 27^\circ\).
What about emitter resistance?

\[ R_e = \frac{N_{be}}{\alpha_e} = \frac{N_{be}}{\alpha} = \frac{\alpha}{g_m} \times \frac{V_t}{I_e} \]

\[ \Rightarrow R_e = \frac{\alpha}{g_m} \times \frac{R}{g_m \times \frac{V_t}{I_e}} \]

Note that although it is not explicitly shown in the hybrid-T model, RE is present.

\[ \Rightarrow \text{i.e., if you analyze this, you find that} \]

To explicitly show emitter resistance, use the T-model:

**T-Model:** (Common Base Model)

- Forward-active

**Small-Signal Model for n-p-n Transistor**

For p-n-p transistors, use the same small-signal models as n-p-n with no change in polarities!

**Hybrid-T Model:**

- Note that in these S.S. models, the same current directions as used for n-p-n are used too
- \( \Rightarrow \text{i.e., no change in S.S. polarities} \)
- (Input signal direction, however, can be as before)
How Complete Hybrid II Model (adding frequency effects of 2\textsuperscript{nd} order effects)

$C_\mu, C_\pi$

**C\_\mu - Base-Collector Capacitance**

- Change models how $\mu$-there are the plates of a capacitor $\rightarrow C_\mu$
- if have $V_{BE} = V_{BE} + V_{BE}$, then $\mu$ gets modulated over small regions
  - thus have one effectively the plates of a capacitor!
- if change to a different bias $V_{BE}$, get new capacitor plate locations $\rightarrow C_{\mu'} = \frac{e^2}{\varepsilon N_x(K_{\pi})}$

$C_\mu = \frac{C_{\mu_0}}{1 + \frac{V_{BE}}{E_0}}$

where $C_{\mu_0} =$ capacitance for $V_{BE} = 0$

$\phi_j =$ function of the built-in potential between $p$ and $n$-type semiconductors

\[
\phi_j \approx \frac{E_0}{q} \ln \left( \frac{N_x N_c}{n_{\pi}^2} \right) \ 	ext{V} \ 	ext{cm}^{-3}
\]

In general:

\[
C_\mu = \frac{C_{\mu_0}}{1 + \frac{V_{BE}}{E_0}} \ 	ext{mF cm}^{-1}
\]

where $m^2 \approx 1$, depending upon how abrupt the junction is

**Detailed Equation:**

\[
\frac{q \phi_j}{\phi_0} = \frac{\left( \frac{2e(K_{\pi} + K_\mu)}{qN_x} \right)^{1/2}}{1 + \frac{V_{BE}}{E_0}} \rightarrow C_\mu = \frac{q \phi_0 N_x K_{\mu}}{A \left( \frac{2eK_{\mu}(K_{\pi} + K_\mu)}{qN_x} \right)^{1/2}} \frac{1}{1 + \frac{V_{BE}}{E_0}}
\]

\[
C_\mu = \frac{eA}{\varepsilon N_x K_{\pi}} \frac{1}{1 + \frac{V_{BE}}{E_0}}
\]

\[
C_{\pi} = \frac{eA}{\varepsilon N_x K_{\pi}} \frac{1}{1 + \frac{V_{BE}}{E_0}}
\]
$C_T$ — Base-to-Emitter Capacitance

Two components comprise $C_T$:  
1. Junction Capacitors, $C_{je}$  
2. Diffusion Capacitors, $C_b$

![Diagram of $C_T$ components]

Diffusion Capacitors: (In Base Charging Capacitance)

- Can define a base transit time:
  \[
  \tau_p = \frac{Q_e}{I_c} = \frac{N_b^2}{2\mu} \text{ avg. time spent by electron in crystal base}
  \]
- Think of $I_c$ as the rate of flow of charge through the base

\[
Q_e = \tau_p I_c
\]

\[
\Delta Q_e = \tau_p \Delta I_c
\]

Switch to S.S. parameters (variable):

\[
\begin{align*}
q_e &= \tau_p I_c \\
q_e &= C_b \frac{V}{N_b} \\
C_T &= \tau_p I_c \\
C_{je} &= \frac{q_e}{V}
\end{align*}
\]

\[
C_T = C_b + C_{je}
\]

\[
C_T = \tau_p I_c + \frac{C_{je}}{1 + \frac{V}{V_b}}
\]

Collector-to-Base Feedback Resistor, $R_{CB}$

Current $I_c = \frac{Q_e}{C_b}$

- $N_{ce}$ $\rightarrow$ $N_{ceB}$ $\rightarrow$ $Q_{eb}$ $\rightarrow$ $I_{ce}$
  
  $I_{ce}$ (due to Early effect)

$N_{ce}$ $\rightarrow$ $I_{ce}$ can be modeled by an $r_o$ current $G_{to-B}$

\[
B \xrightarrow{V_{be}} C \xrightarrow{I_{ce}} N_{ceB}
\]
In general, base recombination current is only part of the total base current
and is the only component dependent on $V_{BE} = \theta$, thus:

$$\alpha \beta V_{BE} R_0 < I_B < \frac{\alpha \beta V_{BE} R_0}{\alpha \beta} \Rightarrow I_B = 2 - 10 \beta V_{BE}$$

(recombination current)

Complete Forward-Active BJT SS Model (including parasitics)

Actual integrated BJT:

Fig. 1.2

P

Substrate
Fig. 1.1
Find \( f_T \) (Early gain freq. for \( \beta \))

\[ f_T \] (early gain freq. for \( \beta \))

Find \( \beta(j\omega) \): (\( \beta \) as a function of freq.)

\[ \beta(j\omega) = \frac{1}{1 + \omega^2 \omega_B^2} \]

Plot \( |\beta(j\omega)| \): (Bode plot)

For \( \omega \) large, \( |\beta(j\omega)| \) close to \( 0 \)

\[ |\beta(j\omega)| = \frac{1}{1 + \omega^2 \omega_B^2} \]

Also, note that \( \omega_T = \omega_B \)

\[ \omega_T = \frac{\omega_T}{C_0 + C_T} \Rightarrow f_T = \frac{\omega_T}{2\pi} \]

\( f_T = 100 \text{ MHz} \rightarrow 15 \text{ GHz} \) for bipolar transistors.

\[ C_T = \frac{g_m}{\omega_T^2} - C_0 \]
MOS Transistors

Physical Structure & Device Symbols
(cross-sectional view) of MOS device
Gate (lychly doped polysilicon)

MOS XJirhr Device Symbols

But first start w/ a perspective view: (this also defines dimension)
-case the n-channel or next page pg (42)

IV Characteristics (NMOS)

Linear: 
\[ I_d \propto \begin{cases} \frac{V_{gs}-V_{th}}{2} & V_{ds} < 2|V_{th}| \\ V_{ds} & V_{ds} > 2|V_{th}| \end{cases} \]

Saturation: 
\[ I_d \propto \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th}^2) V_{ds} \]

MOS XJirhr Mathematical Model

1. Cut-Off Region: \( V_{gs} \leq V_{th} \)
   \[ I_d = 0 ; \quad I_g = 0 \]

2. Linear (or Triode) Region: \( V_{gs} - V_{th} = V_{ds} > 0 \)
   \[ I_g = I_d = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) \frac{V_{ds}}{2} \]

Body Factor: \( \beta = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \) \( V_{ds} \) = substrate doping convection \( k_n (V_{gs} - V_{th} - \frac{V_{ds}}{2}) V_{ds} \)

3. Saturation Region: \( V_{ds} \geq V_{gs} - V_{th} > 0 \)
   \[ I_g = 0 ; \quad I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) \frac{V_{ds}}{2} (1 + \beta V_{ds}) \]
   \[ k_n (V_{gs} - V_{th}) \frac{V_{ds}}{2} (1 + \beta V_{ds}) \]

\[ V_{gs} = f(V_{ds}) = V_{ds} + \frac{1}{2} (V_{gs} - V_{th}) \frac{V_{ds}}{2} \]

\[ \mu_n = \text{mobility of electrons} \]
\[ C_{ox} = \text{gote oxide capacitance per unit area} \]
MOS Transistor Structure

(a) MOS Transistor Diagram

(b) MOS Transistor Circuit Diagram

(c) MOS Transistor Symbol

Fig. 2.1
**PMOS with Mathematical Model**

\[
V_{bs} + \frac{s}{C_{D}} - \frac{V_{gs}}{G} + \frac{1}{C_{L}} + \frac{1}{C_{x}} = V_{ds}
\]

1. **Cut-Off Region**: \(V_{gs} \leq -V_{TP} \) \& \((1V_{gs} \geq 1V_{TP})\)
   \[I_{sd} = 0\]

2. **Linear (or Triode) Region**: \(V_{gs} > -V_{TP} \) \& \((1V_{gs} > 1V_{TP})\)
   \[I_{sd} = \frac{k_{p}}{2} (V_{gs} + V_{TP} - \frac{1}{2})V_{sd} = \frac{1}{2} \mu_{p} C_{ox} \frac{W}{L} (V_{gs} + V_{TP} - \frac{1}{2})V_{sd}\]

For all regions:
   \[k_{p} = \frac{W}{L} \mu_{p} C_{ox} \frac{W}{L}\]

\(I_{g} = 0 \) and \(S = 0\) (at ide)

\[V_{tp} = V_{to} - \frac{1}{2} \left( \frac{1}{V_{gs} + V_{TP} + \sqrt{V_{gs} + V_{TP}} + \sqrt{2V_{TP}}} \right)\]

\(\mu_{p} = \) Hole mobility in the channel

\(C_{ox} = \) gate oxide capacitance per unit area

**Threshold Voltage**

\[V_{t} = \Phi_{mS} - \Phi_{S} - \frac{Q_{B}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}\]

where \(\Phi_{mS}\) = work function difference [in V] between gate material and bulk Si
\(\Phi_{S}\) = surface potential in Ko Si @ onset of strong inversion
   \(\Phi_{S} = 20k_{F} \) for uniformly doped sub strate \((\Phi_{F} = 0.3V)\)

\(Q_{ss}\) = oxide charge per unit area of Ko oxide-Si interface [C/cm²]

\(Q_{B}\) = charge stored per unit area in the depletion region (at onset of inversion)

\[|Q_{B}| = \sqrt{2 \epsilon_{x} \epsilon_{0} N_{A} (2\phi_{F} + 1V_{SS})} [C/cm²]\]

conc. in bulk \(\cap\) reverse bias

\(C_{ox}\) = gate oxide capacitance per unit area [F/cm²]
\[
V_{to} = \phi_{ms} - 2\phi_f - \frac{Q_{ss}}{C_{ox}} - \frac{Q_{bo}}{C_{ox}} - \frac{Q_{bo}}{C_{ox}}, \quad \text{where} \quad \gamma = \sqrt{2q\varepsilon_{Si}N_B(2\phi_f + 1V_{SB})}
\]

Signs in the \( V_t \) Equation:

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<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>p-type</td>
<td>n-type</td>
</tr>
<tr>
<td>( \phi_{ms} ): Metal gate</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>( n+ Si ) gate</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>( p+ Si ) gate</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>( \phi_f )</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>( Q_{bo} ) (or ( Q_b ))</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>( Q_{ss} )</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>( C_{ox} )</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>
MOS Small-Signal Model

Transconductance, $g_m$:

$$g_m = \frac{\partial i_d}{\partial v_{ds}} = \frac{\partial (v_{gs} - v_t)}{\partial v_{ds}}$$

$$g_m = \frac{2}{V_{gs}} \left[ \frac{V_{gs} - V_t}{V_{gs} + 2(V_{gs} + v_{ds} - v_t)} \right]$$

Midband Frequency S.S. Parameters (controlled source and resistor)

Output Resistance, $r_o$:

$$r_o = \frac{1}{g_{ds}}$$

High Frequency S.S. Parameters (capacitors)

$$C_{gd} = \text{gate-to-drain overlap capacitance}$$

$$C_{gs} = \text{gate-to-source overlap capacitance}$$

$$C_{gd} = \frac{1}{\lambda^2 V_{ds}}$$

$$g_{ds} = \frac{1}{2r_o}$$
MOS High Frequency SS Parameters

Gate-to-Source Capacitor, $C_{gs}$:

$$C_{gs} = C_{ox} + \frac{2}{3}WdL_C$$

(inversion charge integrated)

Gate-to-Drain Capacitor, $C_{gd}$:

$$C_{gd} = C_{ox}$$

(no inversion charge near the drain in saturation)

Source/Drain Junction Capacitance, $C_{jox} + C_{jiced}$:

- Some include the poly depletion capacitance associated with the drain-to-bulk and source-to-bulk pn junctions.

- The channel width of the pn junction is different from that at sidewalls due to higher doping at the sidewalls.

- The channel width is reduced as the channel width in the field overlap to prevent channel formation.

- Use as a current-limiting factor.

- $C_{jox}$ is the junction capacitance and $C_{jiced}$ is the depletion capacitance.

- $C_{jox}$ includes the depletion capacitance with $V_{DG} = 0$ and $W = W_{DN}$.

- $C_{jiced}$ includes the depletion capacitance with $V_{DG} = 0$ and $W = W_{DN}$.

- Junction bottom-side area $C_{jox}$ + (junction outside perimeter) $C_{jiced}$

$$C_{jox} + (n+2r)C_{jiced}$$

- $n$ = depletion capacitor, $r$ = sidewall perimeter, $W = W_{DN}$, $L = L_{DN}$.