Lecture 8: Active Loads

- Announcements:
  - No Prof. Nguyen Office Hours on Monday or Thursday next week (on travel)
  - There WILL BE lecture Tuesday, next week
  - But NO LECTURE Thursday, next week???
  - Make-up lecture will probably be Friday in a room and time TBA

- Lecture Topics:
  - Analysis of actively loaded circuits (continued)
  - Current Sources

- Last Time:

Ex. Multistage Active loaded MOS Cft.
\[ T_{o} = (C_{d6} + C_{gd3} + C_{gs4}) \left[ \frac{1}{g_{mv} + g_{mh4}} \right] \]

\[ T_{gs4} = g_{sv4} \left( \frac{(r_{o11} + r_{o2}) + (r_{o3} + r_{o4})}{r_{o4} + g_{mv} + g_{mh4}} \right) \]

From inspection formula \( \frac{2}{g_{mv} + g_{mh4}} \)

but there's a zero, too, in \( M_{o4} \)

\[ W_{t} = \frac{1}{\omega + \omega + \omega + \omega} \]
Get $g_{m1}$, $\frac{N_o}{N_s}$, $\frac{N_o}{N_d}$, $\frac{N_o}{N_2}$

$\frac{N_o}{N_s} = (1)\left(-g_{m1}\left(\frac{1}{g_{md1}+g_{mb2}}\right)\left(g_{m2}+g_{mb2}\right)\right)R_0$

$= -g_{m1}R_0$

Same as C.S., but $R_0 = \text{huge!}$

Get the dominant path (use octree analysis)

As we will see, this node won’t move much! (voltage)

Current source

Note: $V_{gs}$ is a constant.

$V_{gs}$ (input)

$V_{dd}$ (output)

$V_{pin}$ (ground)

If $R_0$ large, $\frac{V_H}{V_{gs}} \approx \frac{1}{R_0}$

$\omega_H = \frac{1}{R_0 + \omega_1 + \omega_2}$

might need to include...

When $R_0$ large

large distance

$\omega_H \approx \frac{1}{R_0}$
Current Sources...
We now focus on methods for generating Vref. But how do we get this degree of precision using a transistor? 

Solution: 

Repetition Biasing (a simple & effective approach) 

1. Generate the desired current. 
2. Push the current through a transistor and allow it to reach a stable bias point. 
3. Use this stable bias point as Vref. 

One simple approach: 

\[ I_{ref} = \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \]

\[ V_{GS} \]

Now, we can distribute this Vref to the gates of many MOS transistor current sources!

Ex. Simple MOS Current Source

\[ V_{DS1} = V_{DS2} \]

In general, 
Diode-connected transistor: saturated: 
\[ I_{D1} = \frac{W}{2L} \left( V_{DS1} - V_{T} \right) \left( V_{GS} - V_{T} \right) \]
\[ I_{D2} = \frac{W}{2L} \left( V_{DS2} - V_{T} \right) \left( V_{GS} - V_{T} \right) \]

1. Case: matched \[ M1 \parallel M2 \Rightarrow I_{D2} = I_{D1} \]
2. Case: \[ M1 \parallel M2 \] scaled up to each other 
\[ \Rightarrow I_{D2} = I_{ref} \left( \frac{W/L_2}{W/L_1} \right) \]
\[ \Rightarrow \text{use } L_1 = L_2 \text{ for both accuracy, then:} \]
\[ \frac{I_0}{I_{ref}} = \frac{W_2}{W_1} \]

Note: For better accuracy, should use multiple copies of one device when scaling currents reduces edge effects!
EE 140: Analog Integrated Circuits
Lecture 8w: Current Sources

Assume $Q_1$ & $Q_2$ are matched.

$$V_{BB1} = V_{BB2} \rightarrow I_{C1} = I_{C2} = I_0 \quad \text{(neglecting } V_{tn})$$

KCL:

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1} \left( 1 + \frac{V}{V} \right)$$

$$\therefore I_{C1} = I_{C2} = I_0 = \frac{I_{ref}}{1 + \frac{V}{V}}$$

and

$$I_{ref} = \frac{V_{ref} - V_{BB1}}{R_{ref}} \Rightarrow R_0 = R_{ref}$$

Again, a single $V_{BB1}$ gen can source many current sources throughout the IC chip:

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} + I_{B3} + \cdots + I_{Bn}$$

$$\therefore I_{C1} \text{ is a single } V_{BB1} \text{ in all cells!}$$

$$I_{C1} = I_{C2} = f(I_{ref})$$

$$KCL \text{ here to get } I_{C2} = I_{ref}$$

$$\Rightarrow I_0 = I_{ref} = \frac{I_{ref}}{1 + \frac{V}{V}}$$

Problem: $\text{error} \sim \frac{V}{V}$ increases as $n$ increases.

$I_0$ directly from $I_{ref}$, and $V$ deviation depends on $n$.

How can one reduce the error?

This was not the case for MOS!
To reduce the error term, use a buffered \( V_{BB} \) generator.

Add a buffer transistor to attenuate the base current from the current source.

This can now drive the base currents of many bipolar transistor current sources (i.e., active loads).

\[
I_{\text{ref}} = I_{10} + I_{\text{BIA}}
\]

\[
I_{\text{BIA}} = \frac{I_{G1} + I_{G2} + \ldots + I_{Gn}}{B+1} = \frac{n I_{G1}}{B+1}
\]

[Assuming identical transistors]

Linear model:

\[
I_{\text{ref}} = I_{10} \left( 1 + \frac{n}{B+1} \right)
\]

Note: Now,

\[
\text{I}_{\text{ref}} = \frac{V_{CC} - 2V_{BE\text{on}}} {R_{\text{ref}}}
\]

Problem: For power saving reasons, oftentimes very small bipolar currents are needed, on the order of \( \mu \text{A} \). This might force you to scale \( \text{I}_{\text{ref}} \) in the above bipolar \( V_{BB} \) generator.

Ex. \( V_{CC} \), \( I_{cc} \), \( I_{E1} = \exp \left( \frac{V_{BE2}}{V_{T}} \right) \)

\[
\text{I}_{\text{E1}} = \frac{I_{cc} \exp \left( \frac{V_{BE2}}{V_{T}} \right)}{I_{E1}}
\]

10x device

\[
\text{I}_{10} = \text{I}_{E1}
\]

\[
\text{I}_{10} = \frac{V_{CC} - V_{BE\text{on}}}{10 R_{\text{ref}}}
\]

\[
R_{\text{ref}} = \frac{20}{I_{cc}} = 600 \text{k}\Omega
\]

(Yes, there's only one transistor on the chip, but this takes up too much space.)

The Low Current Solution: Widlar Current Source

Scale \( I_{cc} = I_{10} \) by reducing \( V_{BB2} \) (relative to \( V_{BB1} \)).

Do this by emitter degenerating \( Q_2 \) via \( R_e \).
\[ V_{BE1} + V_{RE} = V_{BE2} + \frac{1}{2} V_{CE2} = V_{BE1} + V_{CE2} \]

\[ I_{CE2} = V_{BE1} - V_{BE2} \]

\[ I_{CE2} = V_{TH} \ln \frac{I_{CE2}}{I_{ref}} \]

Assuming \( Q_1, Q_2 \) are matched:

\[ I_{CE2} = \frac{I_{ref}}{10} \]

Rule of Thumb:

- \( 1 \mu \text{V} \): \( \frac{1}{10} I_{ref} \)
- \( 4 \mu \text{V} \): \( \frac{1}{5} I_{ref} \)
- \( 60 \mu \text{V} \): \( \frac{1}{10} I_{ref} \)
- \( 120 \mu \text{V} \): \( \frac{1}{50} I_{ref} \)

\[ R_{\text{sh}} \] scale by 1000 using wider spacing

\[ V_{BE1} - V_{BE2} = 120 \mu \text{V} \rightarrow R_e = \frac{120 \mu \text{V}}{5 \mu \text{A}} = 24 \Omega \]

\[ I_{ref} = 500 \mu \text{A} \rightarrow R_{ref} = \frac{20 \mu \text{V}}{500 \mu \text{A}} = 40 \Omega \]

More realistic than 60Ω before.

If want smaller, scale by 1000 indeed.

Another advantage of the wider: larger \( R_e \) is more ideal current source:

\[ R_0 = R_e (1 + \beta) \]

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