PROBLEM SET #8

Issued: Tuesday, Mar. 29th, 2011
Due: Tuesday, April 5th, 2011, 5:00 p.m. in the EE 140 homework box in 240 Cory

1. Design a CMOS output stage based on the circuit of *Fig. PS8.1* to deliver 2 $V_{p\text{-}p}$ (± 1 V) before clipping occurs at the output with R_L = 1 kΩ and $V_{DD} = V_{SS}$ = 2.5 V. Use 10 μA bias current in M_3 and 100 μA idling current in M_1 and M_2. Set $(W/L)_3$ = 50/1 and $(W/L)_6$ = 25/1. Specify the *W/L* for M_1-M_6 that minimizes the total chip area. Use the transistor parameters in the table below. The minimum channel length (L_{drawn}) is 1 μm. Assume the body of each *n*-channel transistor is connected to $-V_{SS}$, and the body of each *p*-channel transistor is connected to V_{DD}. Use SPICE to verify your design by plotting V_o versus V_i.

Parameter	Value	Units
$\left\lvert\frac{dX_d}{dV_{DS}}\right\rvert_n = \lambda_n \cdot L_{eff}$	0.08	$\frac{\mu m}{V}$
$\left\lvert\frac{dX_d}{dV_{DS}}\right\rvert_p = \lambda_p \cdot L_{eff}$	0.04	$\frac{\mu m}{V}$
$2\varphi_{fn}$	0.65	V
$2\varphi_{fp}$	0.75	V
$\lvert V_{t0}\rvert$	0.70	V
γ_n	0.16	$\sqrt{V}$
γ_p	0.43	$\sqrt{V}$
C_{ox}	2.3	$\frac{fF}{\mu m^2}$
L_d	0	μm
μ_n	550	$\frac{cm^2}{V \cdot s}$
μ_p	250	$\frac{cm^2}{V \cdot s}$

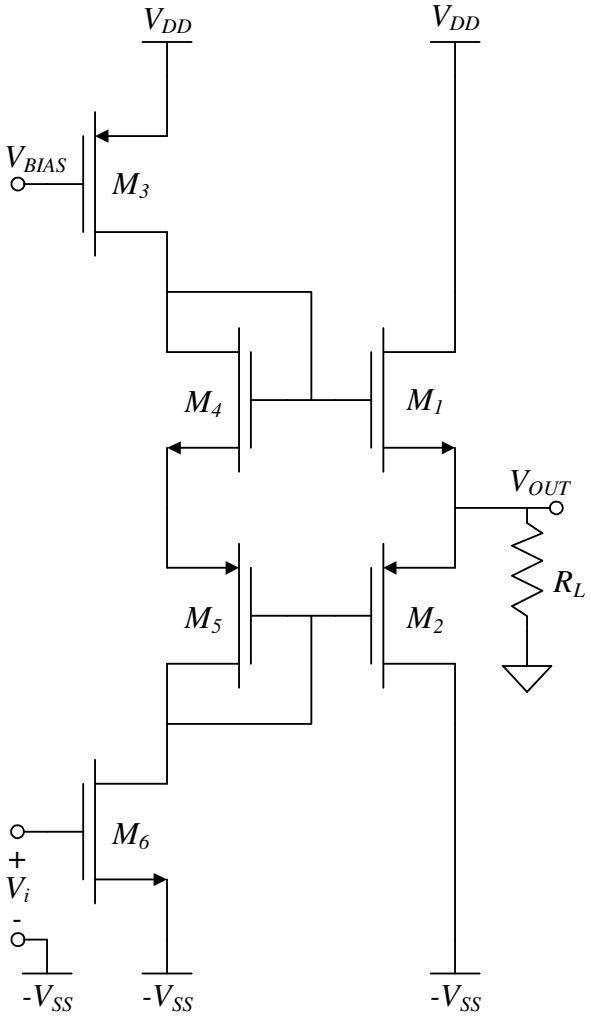

Fig. PS8.1

2. Given the output stage in *Fig. PS8.2a* with input signal $v_{in} = V_x \sin(2\pi f_{in} t)$ and the values below,
   a. Sketch the timing diagrams for one period of $v_{in}(t)$, $v_{out}(t)$, $i_L(t)$, $i_{D1}(t)$, and $i_{D2}(t)$.
   b. Replace R_L in *Fig. PS8.2a* by a capacitive load C_L and repeat part *(a)*.
   c. Now the output stage is connected to an ideal op amp in unity gain feedback as shown in *Fig. PS8.2b*. Sketch the timing diagrams for one period of $v_{in}(t)$, $v_A(t)$, $v_{out}(t)$, $i_L(t)$, $i_{D1}(t)$, and $i_{D2}(t)$.
   d. Replace R_L in *Fig. PS8.2b* by a capacitive load C_L and repeat part *(c)*.

Notes: For each diagram, numerically label peak amplitudes, but only qualitatively show relevant time points. For each part (a, b, c, d), align the time axes (i.e. draw each plot directly below the next). Please be neat in your sketches! Drawing larger helps.

Assumptions: Assume steady state. Neglect all capacitances other than C_L, channel length modulation, body effect, and all other nonidealities. Assume that the input and output are biased around zero volts.

$V_x = 0.6$ V, $f_{in} = 100$ MHz, $C_L = 2$ pF, $R_L = 1$ kΩ,
$V_{OV} = 0.15$ V, $V_t = 0.3$ V, $V_{DD} = V_{SS} = 0.6$ V

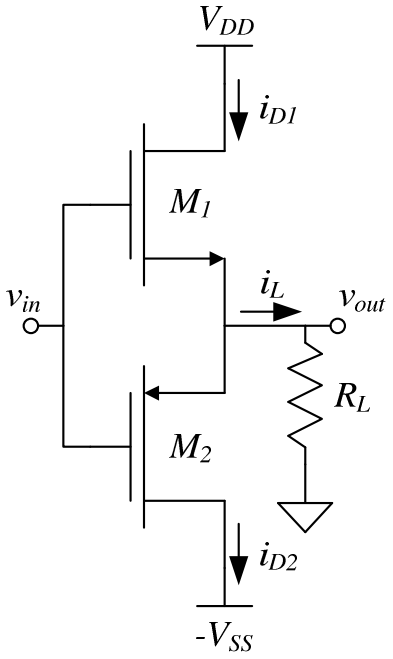

Fig. PS8.2a

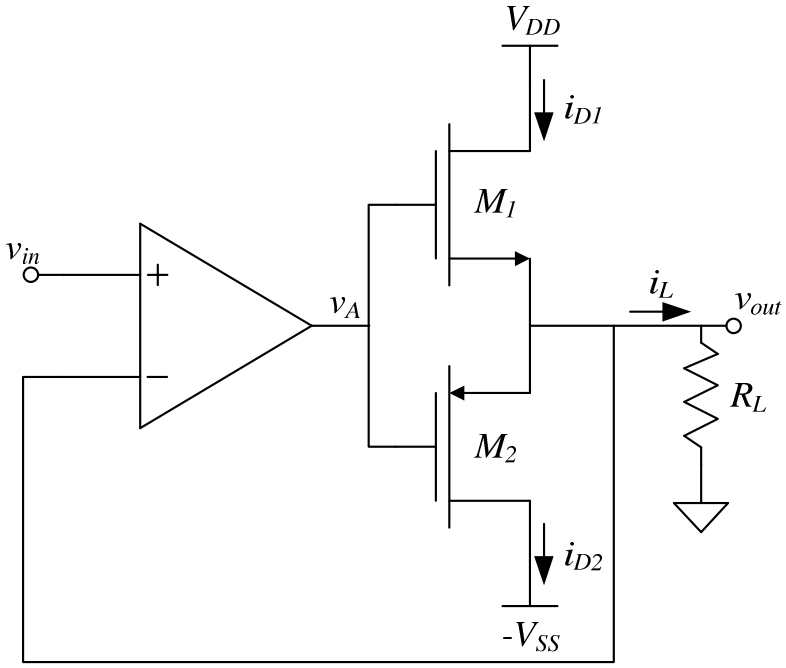

Fig. PS8.2b