PROBLEM SET #6

Issued: Tuesday, Mar. 1st, 2011

Due: Tuesday, Mar. 8th, 2011, 5:00 p.m. in the EE 140 homework box in 240 Cory

1. Design a differential amplifier with an active load as shown in Fig. PS6.1 to meet the following specifications:

   i. Differential gain A_{dm} = 80V/V.

   ii. $I_{REF} = I = 100\mu$A.

   iii. The DC voltage at the gates of M_3 and M_6 is +1.5V.

   iv. The DC voltage at the gates of M_7, M_4 and M_5 is -1.5V.

   M_1 and M_2 form the differential pair while the current source transistor M_4 and M_5 form the active loads for M_1 and M_2 respectively. The DC bias circuit that establishes an appropriate DC voltage at the drain of M_1 and M_2 is neglected here. Use the following technology parameters for your design:

   $\mu_n C_{ox} = 3\mu_p C_{ox} = 90\mu\text{A/V}^2$, $V_{tn} = |V_{tp}| = 0.7$V, $V_{An} = |V_{Ap}| = 20$V

   Your design should include the value of R and the W/L ratio of all transistors. Also specify I_D and $|V_{GS}|$ at which each transistor is operating. For DC bias calculation, you may neglect channel length modulation.

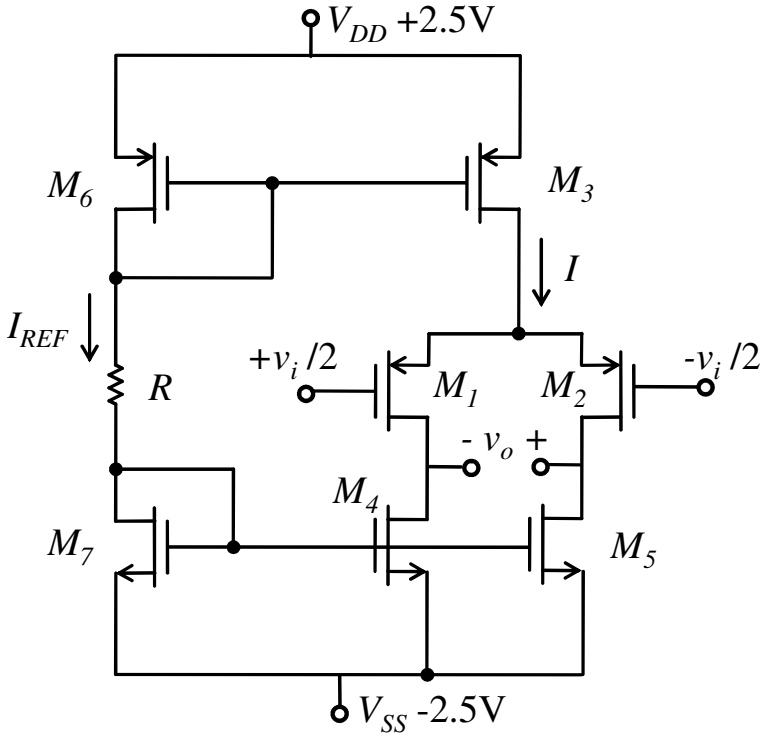

Fig. PS6.1

2. A differential circuit employing active loads is shown in Fig. PS6.2. Bias voltage V_G is adjusted so that the drains of M_1 and M_2 are at +5 V dc. Assume that biasing resistors R_{B1} and R_{B2} set I_{D5} = 1 mA. Calculate the midband small-signal voltage gain v_o/v_i and estimate the dominant pole frequency. Use inspection analysis wherever possible.

   Use the following equations in calculating capacitances:

   $C_{sb} = \frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{\psi_0}}}$

   $C_{db} = \frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{\psi_0}}}$

   $C_{db0} = A_D(C_{j0}) + P_D(C_{jsw0})$, where A_D = (5 μm)W and P_D = W.

   $V_{DD,}$ -V_{SS} = 10 V
   X_d = 1 μm
   γ = 0
   ψ_0 = 0.6 V
   W_1=W_2=W_5=W_6=100 μm
   W_3 = W_4 = 50 μm
   L_{drwn} = 2 μm
   L_d = 0.2 μm
   $\mu_n C_{ox}$ = 60 μA/V^2
   λ_n = 0.1 V^{-1}
   V_{Tn} = 1 V
   C_{ox} = 0.7 fF/μm^2
   $\mu_p C_{ox}$ = 20 μA/V^2
   λ_n = 0.2 V^{-1}
   V_{Tp} = -1 V
   $C_{j0(NMOS)}$ = 0.4 fF/μm^2
   $C_{jsw0(NMOS)}$ = 0.4 fF/um^2
   $C_{j0(PMOS)}$ = 0.2 fF/μm^2
   $C_{jsw0(PMOS)}$ = 0.2 fF/um^2

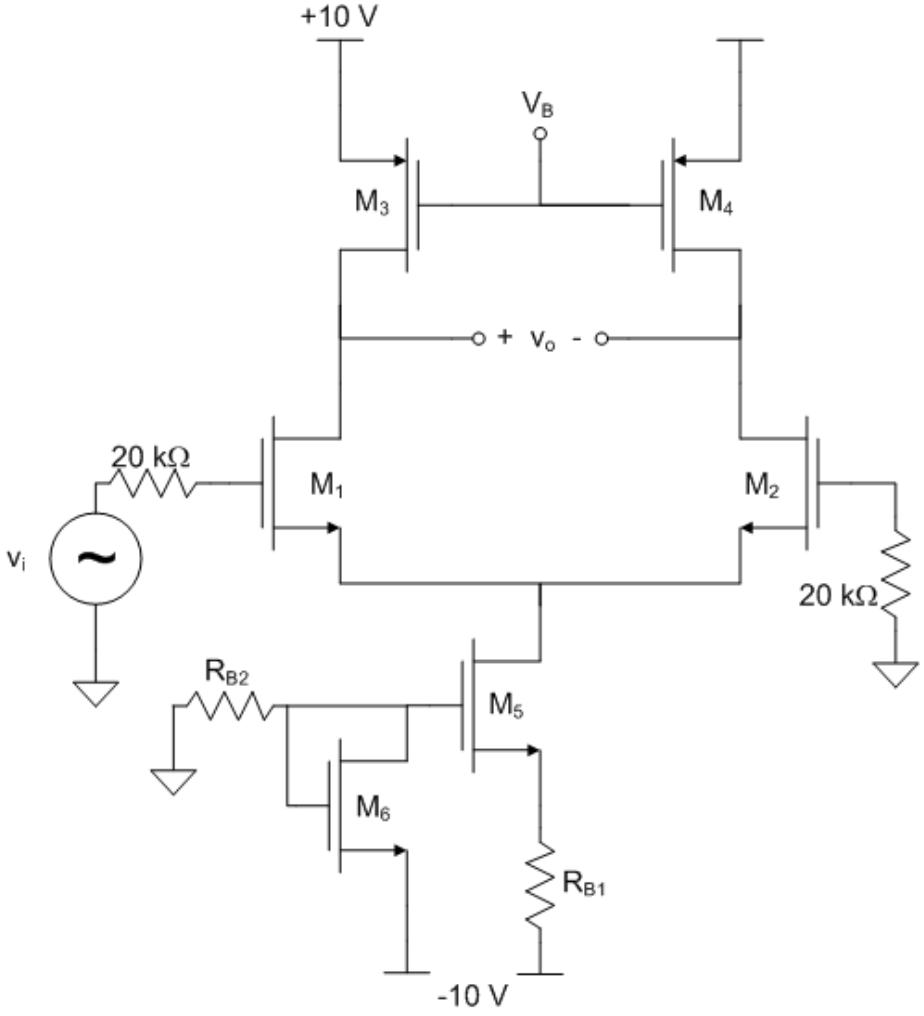

Fig. PS6.2

3. Determine the unloaded voltage gain v_o/v_i and output resistance for the circuit of PS6.3. Check with SPICE and also use SPICE to plot out the large-signal V_O-V_I transfer characteristic for V_{SUP} = 2.5 V. Use SPICE to determine the CMRR if the current-source output resistance is 1 MΩ. Assume no device mismatch. Use the parameters in the table below as necessary.

Parameter		npn	pnp
β_F		200	50
β_R		2	4
V_A		130 V	50 V
η		2e-4	5e-4
I_S		5e-15 A	2e-15 A
I_{CO}		1e-10 A	1e-10 A
BV_{CEO}		50 V	60 V
BV_{CBO}		90 V	60 V
BV_{EBO}		7 V	90 V
τ_F		0.35 ns	30 ns
τ_R		400 ns	3000 ns
β_0		200	50
r_b		200 Ω	300 Ω
r_c *(saturation)*		200 Ω	100 Ω
r_{ex}		2 Ω	10 Ω
C_{je0}	B-E junction	1 pF	0.3 pF
ψ_{0e}		0.7 V	0.55 V
n_e		0.33	0.5
C_{u0}	B-C junction	0.3 pF	1 pF
ψ_{0c}		0.55 V	0.55 V
n_c		0.5 V	0.5
C_{cs0}	C-S junction	3 pF	3 pF
ψ_{0s}		0.52 V	0.52 V
n_s		0.5 V	0.5 V

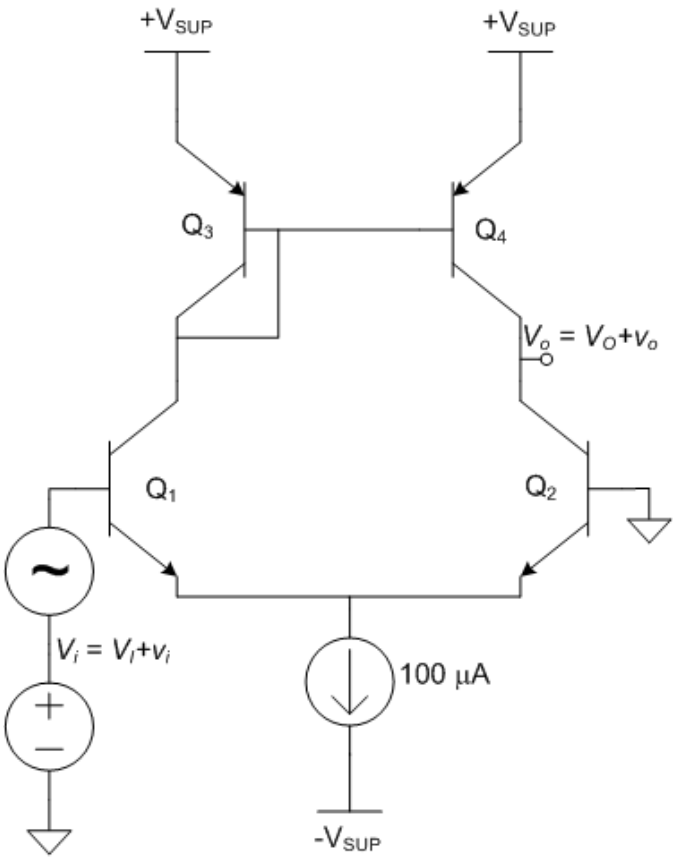

Fig. PS6.3

4. Assuming all of the circuits in show in Fig. PS6.4 are symmetric, all of the transistors are saturated, $\gamma = 0$, and $\lambda \neq 0$,

   i. Calculate the small-signal differential voltage gain of each circuit. You answer should be symbolic in terms of g_{m1}, g_{m2}, g_{m3}, g_{m4}, g_{m5}, r_{o1}, r_{o2}, r_{o3}, r_{o4}, r_{o5}, R_1, R_2. Circuits (a) – (d) can be solved by inspection, but you may need to draw the small signal model to solve (e).

   ii. Sketch V_{out} as V_{in1} and V_{in2} vary differentially from zero to V_{DD}. In other words, plot V_{out} vs. V_{in1}-V_{in2} *(commonly referred to as* V_{id}*)*.

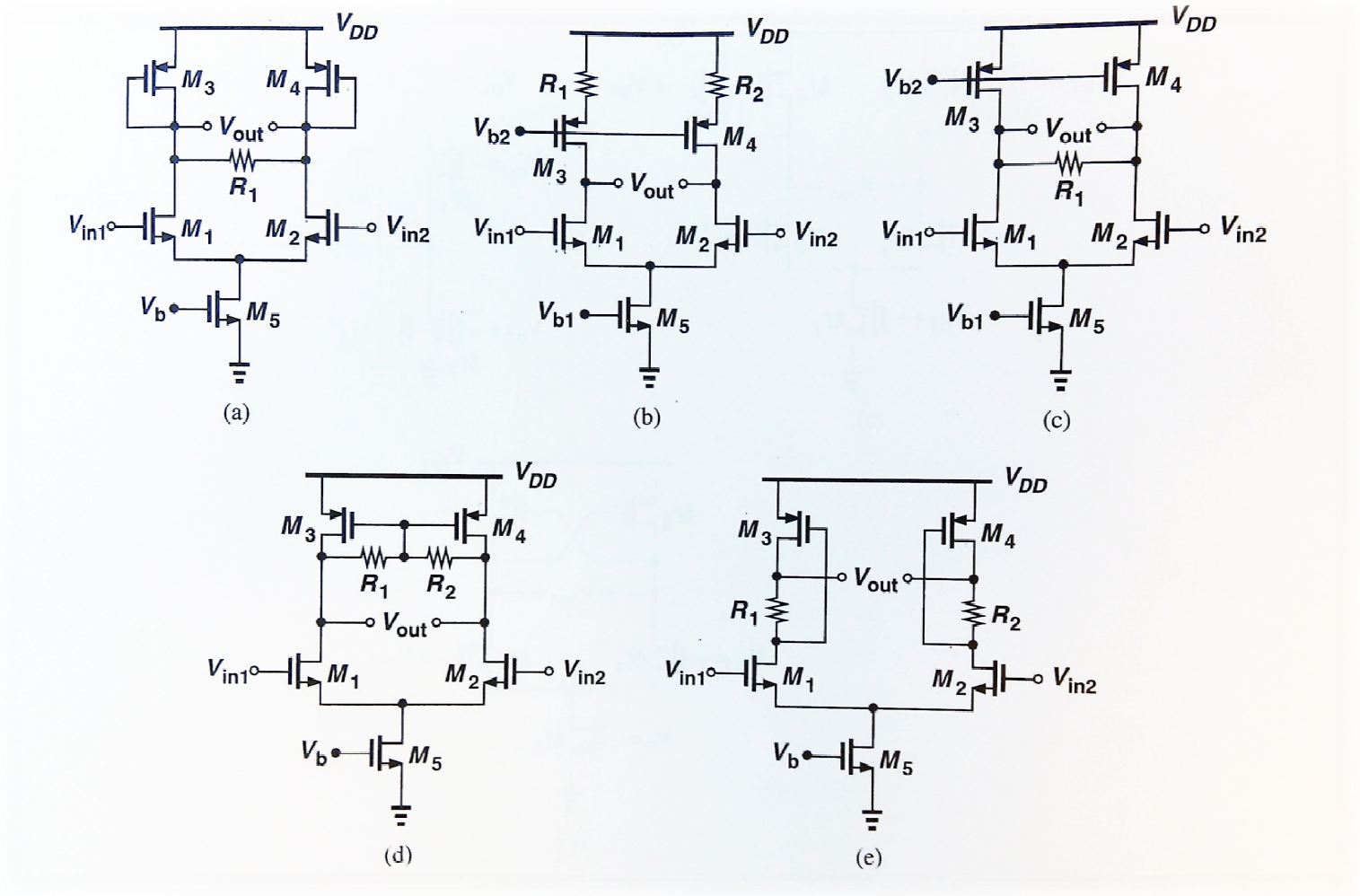

Fig. PS6.4