PROBLEM SET #3

Issued: Tuesday, Feb.8, 2011

Due: Tuesday, Feb.15, 2011, 5:00 p.m. in the EE 140 homework box in 240 Cory

1. Multi-stage analysis

   Fig. PS3.1 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purpose here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.

   a. Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume $|V_{BE}| = 0.7$V, $\beta = 100$, and neglect the Early effect;

   b. Find he input and output resistance;

   c. Use the current-gain method to evaluate the voltage gain vo/vi;

   d. Find the high frequency pole formed at the interface between the first and the second stages. Assume that $C_{\mu 2} = 2$pF and $C_{\pi 2} = 10$pF.

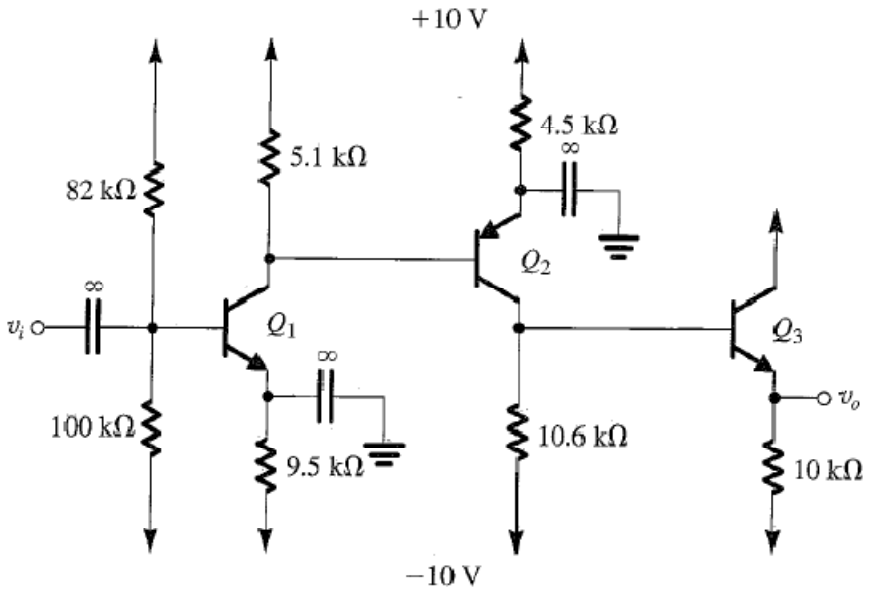

Fig. PS3.1

2. Cascode stage analysis

   The ac schematics of a common-source stage and a cascode stage are shown in Fig. PS3.2 with R_S = 10 kΩ and R_L = 20 kΩ. Using the transistor and operating point data below,

   a. Calculate the low-frequency, small signal voltage gain v_o/v_i for each circuit.

   b. Calculate the -3 dB frequencies of the two circuits.

   Data: I_D = 0.5 mA, W = 100 μm, L_{drwn} = 2 μm, L_d = 0.2 μm, X_d = 0, λ = 0, k'_n = 60 μA/V^2, γ = 0, $C_{sb} = C_{db}$ = 0, C_{ox} = 0.7 fF/μm^2, and C_{gd} = 14 fF.

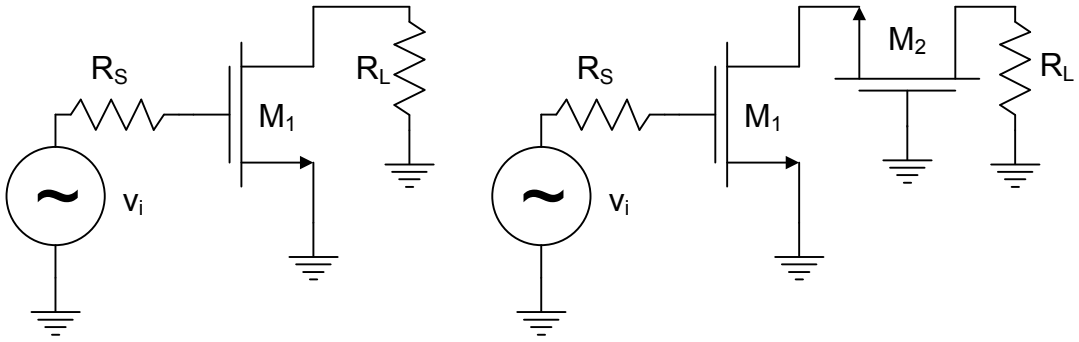

Fig. PS3.2

3. Single-stage design

   Use the following parameters:

$\mu_n C_{ox}$ = 100 μA/V^2	$\mu_p C_{ox}$ = 50 μA/V^2	V_T = 0.5 V	V_{DD} = 3 V
L = 1 μm	$W_p = 2\ W_n$	$(V_{GS} - V_T)_{min}$ = 100 mV for strong inversion	
C_L = 4 pF	C_{gs} = 1 pF	C_{gd} = 0 pF	C_{db} = 1 pF

   a. What is the maximum midband voltage gain of a resistively loaded common source amplifier operating in strong inversion? Use $\lambda_{n,p} = 0$.

   b. How about with an active (PMOS) load? $\lambda_{n,p}$ = 0.1 V^{-1}.

   c. If I_D = 1 mA, how would you size each of the devices?

   d. With I_D = 1 mA, what is the dominant pole frequency of each of these amplifiers?

4. PNP-input active load stage analysis

   An amplifier is shown in Fig. PS3.4. I_B is adjusted such that $V_O = 0$ V dc. $V_{SUPPLY} = 10$ V. Calculate the low-frequency, small signal transresistance v_o/v_i, and estimate the -3 dB frequency.

   npn:

   $\beta = 100$, $f_T = 500$ MHz at $I_C = 1$ mA, $C_{\mu 0} = 0.7$ pF, $C_{je} = 3$ pF (at the bias point), $C_{cs0} = 2$ pF, $r_b = 0$, and $V_A = 120$ V. Assume $n = 0.5$ and $\psi_0 = 0.55$ V for all junctions.

   pnp:

   $\beta = 50$, $f_T = 4$ MHz at $I_C = -0.5$ mA, $C_{\mu 0} = 1.0$ pF, $C_{je} = 3$ pF (at the bias point), $C_{bs0} = 2$ pF, $r_b = 0$, and $V_A = 50$ V. Assume $n = 0.5$ and $\psi_0 = 0.55$ V for all junctions.

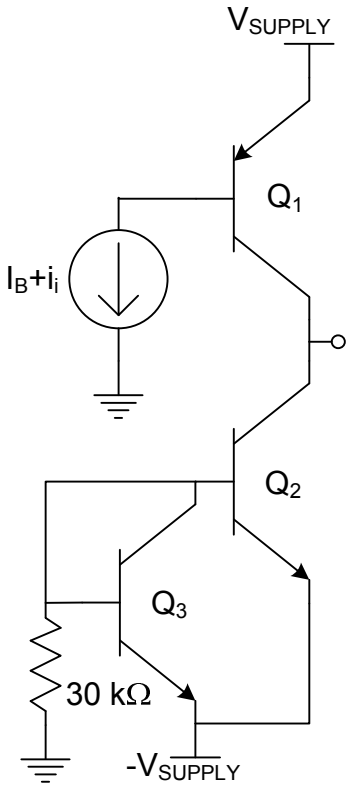

Fig. PS3.4