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PROBLEM SET #11

Issued: Tuesday, Apr. 19th, 2011
Due: Tuesday, Apr. 26th, 2011, 5:00 p.m. in the EE 140 homework box in 240 Cory

1. In the two stage op amp of Fig. PS11.1, $W/L_{1\text{-}4}$ = 50/0.5. Also, I_{ss} = 0.25 mA and each output branch is biased at 1mA. V_{DD} = 3V and use the parameters in the table below.

NMOS Model			
LEVEL = 1	VTO = 0.7V	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08μm	μ_n = 350cm^2/Vs	λ_n = 0.1 V$^{1/2}$
TOX = 9nm	PB = 0.9V	CJ = 0.56e-3 F/m^2	CJSW = 0.35e-11 F/m
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e-9 F/m	JS = 1.0e-8 A/m^2
PMOS Model			
LEVEL = 1	VTO = -0.8V	GAMMA = 0.4	PHI = 0.9
NSUB = 5e+14	LD = 0.09μm	μ_p = 100cm^2/Vs	λ_p = 0.2 V$^{1/2}$
TOX = 9nm	PB = 0.9V	CJ = 0.94e-3 F/m^2	CJSW = 0.32e-11 F/m
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9 F/m	JS = 0.5e-8 A/m^2

a) If a maximum output swing of 0.4~2.4V is desired, design $W/L_{5\text{-}8}$.
b) Determine the CM level at nodes X and Y using the $W/L_{5,6}$ = 60/0.5 and $W/L_{7,8}$= 50/0.5. Use these sizings for all the problems below.
c) If each output is loaded by a 1-pF capacitor, compensate the op amp by Miller capacitors C_c across the gates and drains of $M_{5,6}$ for a phase margin of 60^o in unity-gain feedback. Calculate the pole and zero positions after compensation.
d) Design the resistance that must be placed in series with the compensation capacitors to position the zero atop the non-dominant pole.
e) Determine the slew rate.

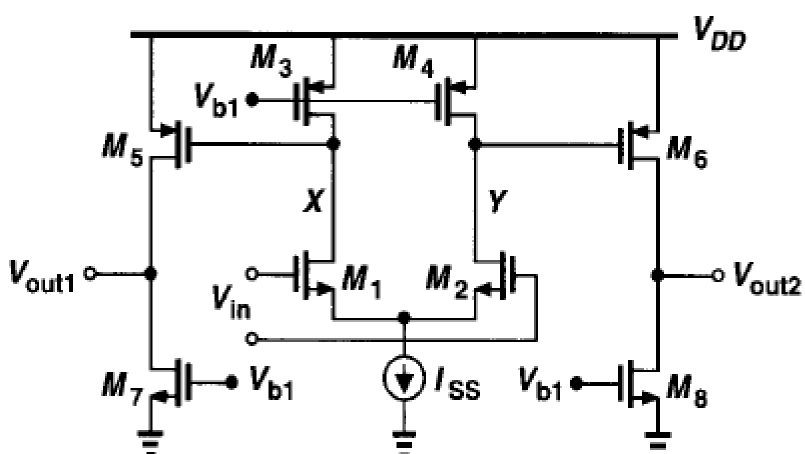

Fig. PS11.1