1) Design a CMOS folded cascode op-amp with the following specs:
   - Input common mode range includes the top rail
   - Output swing to within 300mV of both rails
   - 100uA drain current in all transistors in the signal path
   - 5V single-sided supply
   - all channels are 1um
   You may use one resistor in the bias circuit for your design. All other devices must be transistors. Use cascoded current sources in your bias network to minimize current variation in the different legs.

Draw your amplifier and it’s complete bias circuit. Maybe draw it on scratch paper first so that you can draw it neatly here!

Assume that the input common mode is biased at 2.5V, and label all node voltages and all branch currents.

For each device (or pair of devices if they are identical) in your design, calculate the device width, drain current, saturation voltage, transconductance, and output resistance.

<table>
<thead>
<tr>
<th>name</th>
<th>W</th>
<th>I_d</th>
<th>V_{DSAT}</th>
<th>g_m</th>
<th>r_o</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 L/R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

What is the output impedance of your op-amp?
What is the gain of your op-amp?

Hints: start with ideal voltage biases first to make sure that the amplifier works, then build your real bias network.
2) Simulate your amplifier with the same common mode input as above, and make a table comparing the simulated currents and hand-calculated currents. Do an AC analysis - what is the phase margin of the unloaded op-amp? How much output capacitance is needed to make the amplifier stable in unity gain (e.g. with a phase margin of 45)?

3) Use spice to simulate the voltage drop across the following three elements at the following four temperatures: -40, 0, 25, 85 centigrade.
   - Three diodes in parallel with 1mA total flowing through them
   - Single diode with 1mA flowing through it
   - Single diode with 3mA flowing through it
Plot the voltages vs. temperature. What’s the temperature coefficient? Are they all the same? Why?
Plot the differences between these voltages vs. absolute temperature. Are they PTAT? Compare your simulated results with hand calculations.

4) Implement the circuit in Figure 4.46C in GHLM using an “E” element for the opamp with a gain of 1,000. Let R3=100Ohms. Let R1=R2= 25*R3 initially. This will probably give too much positive temperature dependence. Make a scratch plot of the output voltage of the opamp, vs. absolute temperature. Do you have a positive temperature coefficient, or negative? Change the resistor ratio from 25 to whatever it takes to get a nice flat output voltage. I got mine to only 1mV of variation from -40 to +85C. Plot the output voltage of the opamp, the voltage on D2, the voltage across R3, and the voltage across R2, as a function of absolute temperature.
5) Could you use your op-amp from problem 1 in place of the ideal amplifier above? Why, or why not? How about your amplifier from project 1?

Some helpful info:
k_BT/q at 300C is 25.8mV
k_BT is 86uV/K
ln(3)= 1.1
0K = -273 C
300K = 27C is approximately room temperature (a little warm, just over 80F for those who like British units)

* bandgap w/ ideal amp
* use the standard spice diode model, no changes
.model subDiode D

* “m=3” means put down 3 copies in parallel
d1 d1 0 subDiode
d2 d2 0 subDiode m=3

* these resistors all have a positive temperature coefficient of 0.1%/K
r1 out d1 2.5k tc=0.001
r2 out minus 2.5k tc=0.001
r3 minus d2 100 tc=0.001

* ideal opamp, but with a gain of 1000
eamp out 0 d1 minus 1000
* this forces spice away from the "all voltages=0" equilibrium solution
ibias out 0 -1u

* this tells spice to simulate at 4 different temperatures
.temp -40, 0, 25, 85
.options post
.op
.end