

EECS140
Fall 2009 2008
HW2

Due 8/10/09, 8am, in the box on the 2nd floor

1. The Microlab on the 4th floor of Cory Hall is arguably the world's greatest research clean room. While we sometimes hold the record for the smallest or the fastest transistors in the world, there is also a regular "standard" CMOS run for characterization purposes. The report from a recent run is available online at: <http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-168.pdf> Looking at section 4.2, you can see some of the measured results from this run. As you make the estimates below, spend some time thinking about the best method to make the estimate, but don't worry too much about accuracy.
 - a. From Figure 5, estimate k' for the NMOS and PMOS devices.
 - b. From Figure 5, estimate the threshold voltage of the NMOS and PMOS devices as a function of the source to bulk voltage. What is V_{t0} , and what's a rough estimate for γ for these devices?
 - c. From Figure 6, what's a rough estimate of the transconductance per amp, g_m / I_d , of the NMOS devices in the weak inversion, sub-threshold region? Roughly what is the range of currents for which the NMOS device is in weak inversion? What does that mean about the range of transconductance?
 - d. From Figure 7, plot the saturation drain current vs. the gate voltage. Does this look like a quadratic device?
 - e. From Figure 7, estimate the output resistance in saturation when V_g is two or three volts. Estimate λ .
 - f. From Figure 8, what's a rough estimate of the percentage variation in V_t from die to die? It's common for device parameters like V_t to vary linearly with position across a wafer. Do you see that in Appendix C?
2. Intel's latest 32nm technology was presented at the IEDM conference recently: <http://www.intel.com/technology/architecture-silicon/32nm/32nm.htm>. Using Figure 5 in this paper,
 - a. estimate g_m and r_o for the NMOS and PMOS devices when V_{gs} is 0.7V.
 - b. What would the gain be if I made an NMOS common source amplifier out of this device, using a perfect current source load?
 - c. What would the gain be for an NMOS common source amplifier with a PMOS load using these devices? Assume a 1V supply, and a PMOS bias voltage of 0.4V.
3. Using the standard ee140 0.5um CMOS process models, assume that you want to design a transistor to have a transconductance $g_m = 1\text{mS}$. You may also ignore the effect of λ (assume it's zero for this problem only)
 - a. If you pick the current through the transistor to be 1mA, what will the overdrive voltage and the W/L ratio be if the device is NMOS? PMOS?
 - b. If you pick the overdrive voltage $V_{ov} = 200\text{mV}$, what will the current and W/L ratio be if the device is NMOS? PMOS?
 - c. If you fix the geometry to be 50u/0.5u, what will the current and overdrive voltage be if the device is NMOS? PMOS?

- d. What is the minimum current that will give me this transconductance in any device in this process? What device type (N or P), overdrive voltage, and size will that correspond to?
 - e. What is the smallest device that can have this transconductance?
4. Draw an RC low pass filter with a 10k resistor and a 100fF capacitor.
- a. What is the time constant τ of this filter? What is the angular frequency ω_c (radians/second) at which the capacitor has the same magnitude of impedance as the resistor? What is the pole frequency f_c (Hz)? How are these terms related?
 - b. Draw by hand a cycle or two of the input and output voltages of this filter when driven by a 1V amplitude sine wave with 3 different frequencies: $\{0.1, 1, 10\} * f_c$. Concentrate on getting the phase and amplitude correct.
 - c. Draw by hand a cycle or two of the input and output voltages of this filter when driven by a 1V amplitude square wave with the same frequencies. Concentrate on getting the slope correct at the rising and falling edges of the input.
5. For the common source NMOS amplifier with a PMOS load shown below,
- a. Calculate the current flowing in the PMOS device when the output is at mid-rail (1.5V). You must take channel length modulation into account.
 - b. Calculate the gate bias needed on the NMOS device to keep the output at mid-rail.
 - c. Calculate $g_m, r_o, C_{gs}, C_{gd}, C_{db}$ for each transistor at this bias point. Are both devices in saturation?
 - d. Use the .op command to get SPICE to calculate the same parameters, and compare your answers with what SPICE calculates, showing percent error.

