designs besides opamps. The next subsection will show how it can be incorporated into the constant g_m bias circuit described in Chapter 5.

Wide-Swing Constant-Transconductance Bias Circuit

It is possible to incorporate wide-swing current mirrors into the constant-transconductance bias circuit described in Chapter 5. This modification greatly minimizes most of the detrimental second-order imperfections caused by the finite-output impedance of the transistors, without greatly restricting signal swings. The complete circuit is shown in Fig. 6.2. This circuit is a modification of the circuit described in Fig 5.10, and has both wide-swing current mirrors and a start-up circuit.

The n-channel wide-swing cascode current mirror consists of transistors Q_1–Q_4, along with the diode-connected biasing transistor Q_5. The pair Q_3, Q_4 acts similarly to a diode-connected transistor at the input side of the mirror. The output current comes from Q_1. The gate voltages of cascode transistors Q_1 and Q_4 are derived by the diode-connected transistor Q_5. The current for this biasing transistor is actually derived from the bias loop via Q_{10} and Q_{11}.

Similarly, the p-channel wide-swing cascode current mirror is realized by Q_6–Q_9. Transistors Q_8 and Q_9 operate as a diode-connected transistor at the input side of the mirror. The current-mirror output current is the drain current of Q_6. The cascode transistors Q_6 and Q_9 have gate voltages derived from diode-connected Q_{14}, which has a bias current derived from the bias loop via Q_{12} and Q_{13}.

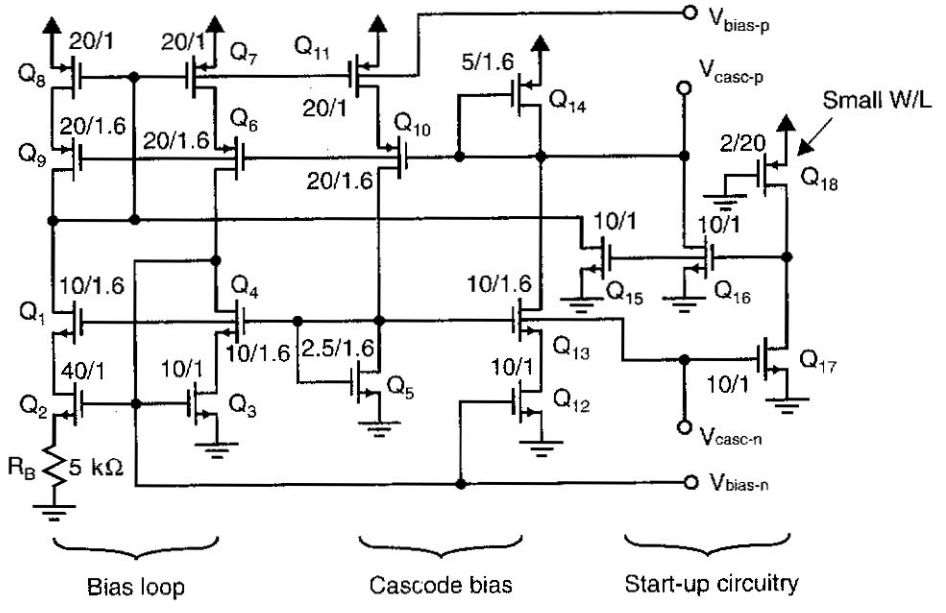

Fig. 6.2 A constant-transconductance bias circuit having wide-swing cascode current mirrors.

The bias loop does have the problem that at start-up it is possible for the current to be zero in all transistors, and the circuit will remain in this stable state forever. To ensure this condition does not happen, it is necessary to include start-up circuitry that affects only the bias-loop in the case that all currents in the loop are zero. An example of a start-up circuit consisting of transistors Q_{15}, Q_{16}, Q_{17}, and Q_{18} is also shown in Fig. 6.2. In the event that all currents in the bias loop are zero, Q_{17} will be off. Since Q_{18} operates as a high-impedance load that is always on, the gates of Q_{15} and Q_{16} will be pulled high. These transistors then will inject currents into the bias loop, which will start up the circuit. Once the loop starts up, Q_{17} will come on, sinking all of the current from Q_{18}, pulling the gates of Q_{15} and Q_{16} low, and thereby turning them off so they no longer affect the bias loop. This circuit is only one example of a start-up loop, and there are many other variations. For example, sometimes the p-channel transistor, Q_{18}, is replaced by an actual resistor (perhaps realized using a well resistor).

It is of interest to note that the bias circuit shown consists of four different loops—the main loop with positive feedback, the start-up loop that eventually gets disabled, and the two loops used for establishing the bias voltages for the cascode transistors. These latter two loops also constitute positive feedback but with very little gain.

Shown next to each transistor are reasonable W/L dimensions (in μm) of a possible realization that had its operation experimentally verified (it was realized in a 0.8-μm technology). Because this circuit allowed for accurately predictable transconductances, it also allows the performance of the realized opamp to be accurately predicted using moderately simple equations prior to realization.

Enhanced Output-Impedance Current Mirrors

Another variation on the cascode current mirror is often referred to as the *enhanced output-impedance current mirror*. A simplified form of this circuit is shown in Fig. 6.3, and it is used to increase the output impedance. The basic idea is to use a feedback amplifier to keep the drain-source voltage across Q_2 as stable as possible, irrespective of the output voltage. The addition of this amplifier ideally increases the

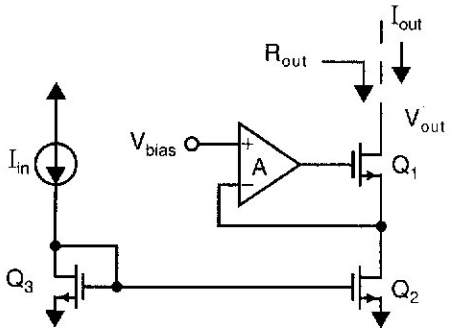

Fig. 6.3 The enhanced output-impedance current mirror.