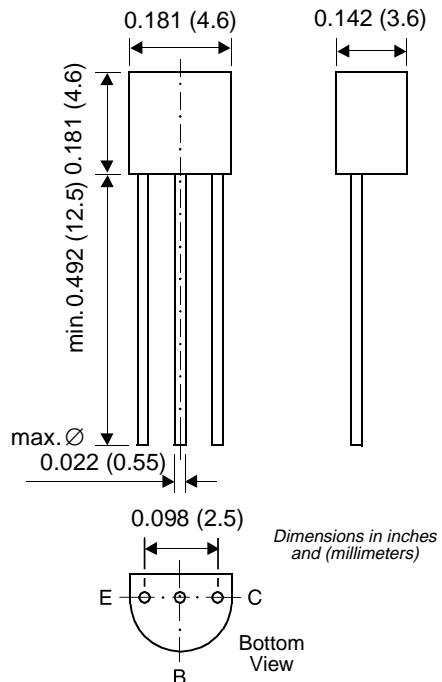




## Small Signal Transistor (NPN)

**TO-226AA (TO-92)**



### Features

- NPN Silicon Epitaxial Planar Transistor for switching and amplifier applications.
- As complementary type, the PNP transistor 2N3906 is recommended.
- On special request, this transistor is also manufactured in the pin configuration TO-18.
- This transistor is also available in the SOT-23 case with the type designation MMBT3904.

### Mechanical Data

**Case:** TO-92 Plastic Package

**Weight:** approx. 0.18g

**Packaging Codes/Options:**

E6/Bulk - 5K per container

E7/4K per Ammo tape

### Maximum Ratings & Thermal Characteristics

Ratings at 25°C ambient temperature unless otherwise specified.

Parameters		Symbols	Value	Units
Collector-Emitter Voltage		V <sub>C EO</sub>	40	V
Collector-Base Voltage		V <sub>C BO</sub>	60	V
Emitter-Base Voltage		V <sub>E BO</sub>	6.0	V
Collector Current		I <sub>C</sub>	200	mA
Power Dissipation	T <sub>A</sub> = 25°C T <sub>c</sub> = 25°C	P <sub>tot</sub>	625 1.5	mW W
Thermal Resistance Junction to Ambient Air		R <sub>θJA</sub>	250 <sup>(1)</sup>	°C/W
Junction Temperature		T <sub>j</sub>	150	°C
Storage Temperature Range		T <sub>s</sub>	- 65 to +150	°C

**Notes:**

(1) Valid provided that leads are kept at ambient temperature.

## Small Signal Transistor (NPN)

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	$V_{(\text{BR})\text{CBO}}$	$I_C = 10 \mu\text{A}, I_E = 0$	60	—	—	V
Collector-Emitter Breakdown Voltage <sup>(1)</sup>	$V_{(\text{BR})\text{CEO}}$	$I_C = 1 \text{ mA}, I_B = 0$	40	—	—	V
Emitter-Base Breakdown Voltage	$V_{(\text{BR})\text{EBO}}$	$I_E = 10 \mu\text{A}, I_C = 0$	6	—	—	V
Collector Saturation Voltage	$V_{\text{CEsat}}$	$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$ $I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$	— —	— —	0.2 0.3	V
Base Saturation Voltage	$V_{\text{BEsat}}$	$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$ $I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$	— —	— —	0.85 0.95	V
Collector-Emitter Cutoff Current	$I_{\text{CEV}}$	$V_{\text{EB}} = 3 \text{ V}, V_{\text{CE}} = 30 \text{ V}$	—	—	50	nA
Emitter-Base Cutoff Current	$I_{\text{EBV}}$	$V_{\text{EB}} = 3 \text{ V}, V_{\text{CE}} = 30 \text{ V}$	—	—	50	nA
DC Current Gain	$\text{h}_{\text{FE}}$	$V_{\text{CE}} = 1 \text{ V}, I_C = 0.1 \text{ mA}$ $V_{\text{CE}} = 1 \text{ V}, I_C = 1 \text{ mA}$ $V_{\text{CE}} = 1 \text{ V}, I_C = 10 \text{ mA}$ $V_{\text{CE}} = 1 \text{ V}, I_C = 50 \text{ mA}$ $V_{\text{CE}} = 1 \text{ V}, I_C = 100 \text{ mA}$	40 70 100 60 30	— — 300 — —	— — — — —	—
Input Impedance	$\text{h}_{\text{ie}}$	$V_{\text{CE}} = 10 \text{ V}, I_C = 1 \text{ mA}$ $f = 1 \text{ kHz}$	1	—	10	k $\Omega$
Voltage Feedback Ratio	$\text{h}_{\text{re}}$	$V_{\text{CE}} = 10 \text{ V}, I_C = 1 \text{ mA}$ $f = 1 \text{ kHz}$	$0.5 \cdot 10^{-4}$	—	$8 \cdot 10^{-4}$	—
Gain-Bandwidth Product	$f_T$	$V_{\text{CE}} = 20 \text{ V}, I_C = 10 \text{ mA}$ $f = 100 \text{ MHz}$	300	—	—	MHz
Collector-Base Capacitance	$C_{\text{CBO}}$	$V_{\text{CB}} = 5 \text{ V}, f = 100 \text{ kHz}$	—	—	4	pF
Emitter-Base Capacitance	$C_{\text{EBO}}$	$V_{\text{CB}} = 0.5 \text{ V}, f = 100 \text{ kHz}$	—	—	8	pF
Small Signal Current Gain	$\text{h}_{\text{fe}}$	$V_{\text{CE}} = 10 \text{ V}, I_C = 1 \text{ mA},$ $f = 1 \text{ kHz}$	100	—	400	—
Output Admittance	$\text{h}_{\text{oe}}$	$V_{\text{CE}} = 1 \text{ V}, I_C = 1 \text{ mA},$ $f = 1 \text{ kHz}$	1	—	40	$\mu\text{S}$
Noise Figure	NF	$V_{\text{CE}} = 5 \text{ V}, I_C = 100 \mu\text{A},$ $R_G = 1 \text{ k}\Omega, f = 10 \dots 15000 \text{ kHz}$	—	—	5	dB
Delay Time (see fig. 1)	$t_d$	$I_{B1} = 1 \text{ mA}, I_C = 10 \text{ mA}$	—	—	35	ns
Rise Time (see fig. 1)	$t_r$	$I_{B1} = 1 \text{ mA}, I_C = 10 \text{ mA}$	—	—	35	ns
Storage Time (see fig. 2)	$t_s$	$-I_{B1} = I_{B2} = 1 \text{ mA}$ $I_C = 10 \text{ mA}$	—	—	200	ns
Fall Time (see fig. 2)	$t_f$	$-I_{B1} = I_{B2} = 1 \text{ mA}$ $I_C = 10 \text{ mA}$	—	—	50	ns

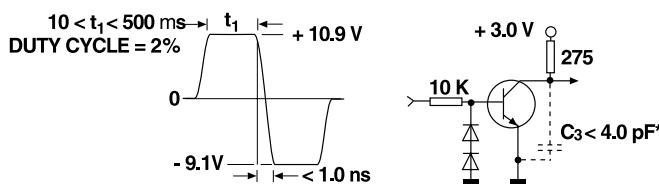


Fig. 1: Test circuit for delay and rise time  
\* total shunt capacitance of test jig and connectors

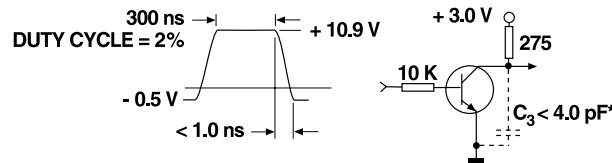


Fig. 2: Test circuit for storage and fall time  
\* total shunt capacitance of test jig and connectors