Small-signal model

* No OH today
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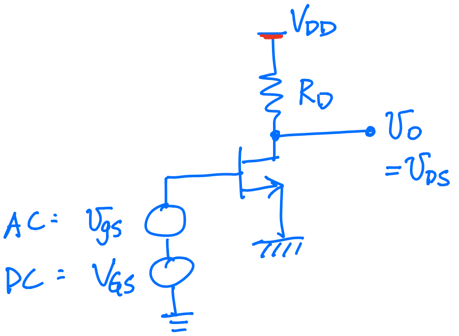
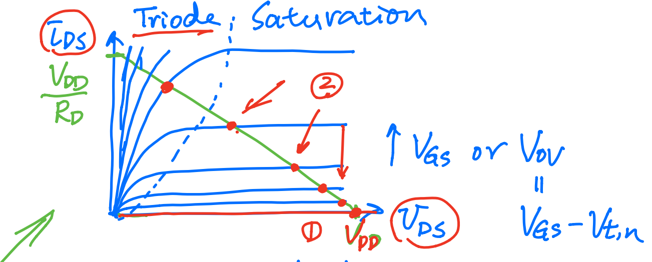


Graphic solution



Load Line → KVL

$$V_{DD} = \boxed{i_D} R_D + \boxed{v_{DS}}$$

EE16A/B : Digital operation

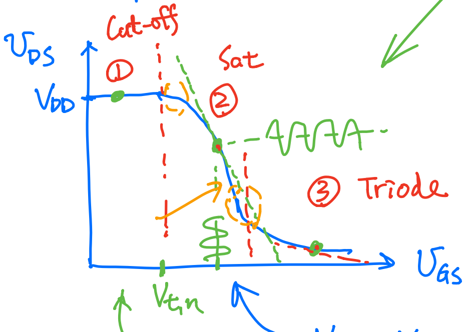
Inverter : ① cut-off → "1"

③ Triode → "0"

EE105 : Analog operation

Amplifier : ② Saturation

Transfer characteristics
(Output-vs-input)



$V_{GS} < V_{t,n}$

Cut-off, $i_D = 0$

$v_O = V_{DD} - i_D \cdot R_D = V_{DD}$

$V_{GS} > V_{t,n}$, $v_O = V_{DD} - i_D \cdot R_D$, NMOS in saturation

$= V_{DD} - \frac{1}{2} k_n V_{ov}^2 \cdot R_D$

$= V_{DD} - \frac{1}{2} k_n (V_{GS} - V_{t,n})^2 \cdot R_D$

Amplifier

$$v_O = V_{DD} - \frac{1}{2} k_n (v_{GS} - V_{t,n})^2 \cdot R_D$$

ac input

ac output $\rightarrow \underline{v_{ds}} + V_{DS} = V_{DD} - \frac{1}{2} k_n (V_{GS} + \underline{v_{gs}} - V_{t,n})^2 \cdot R_D$

Solve DC first : $V_{DS} = V_{DD} - \frac{1}{2} k_n (V_{GS} - V_{t,n})^2 R_D$

Voltage gain

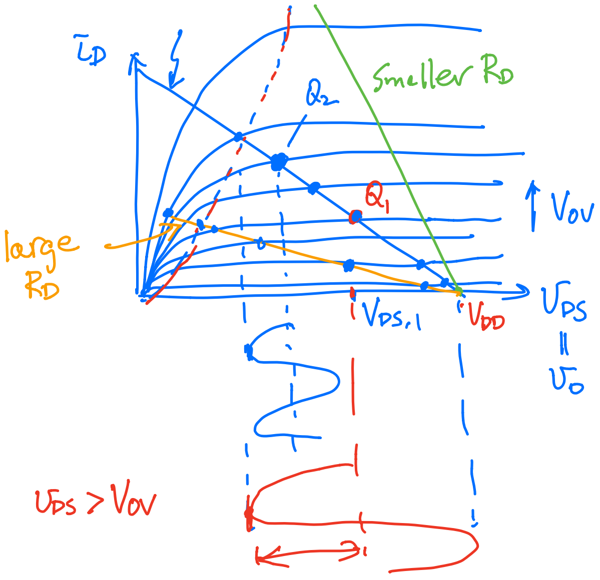
Negative

$$A_v = \left.\frac{\partial v_{ds}}{\partial v_{gs}}\right|_Q = -k_n (V_{GS} - V_{t,n}) R_D = -\underset{\uparrow}{k_n} \overset{\uparrow}{\underset{\downarrow}{V_{ov}}} \overset{\downarrow}{\underset{\uparrow}{R_D}} \Leftarrow$$

$\mu_n C_{ox}\left(\frac{W}{L}\right)$

↑
Bias point
$v_{GS} = V_{GS}$ (i.e, $v_{gs} = 0$)

Slope $= \frac{1}{R_D}$

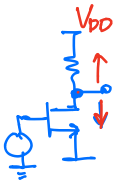


For large A_v

- Bias at high V_{GS} → V_{OV}
  e.g. bias at Q_2
  → Sacrafice output voltage swing
- Q_1 is better Q_2 for swing
- Increase R_D
  → Use lower V_{GS}, or V_{OV}

To stay in small-signal
input signal constraint
Need $v_{DS} \geq v_{OV} = v_{GS} - V_{t,n}$

maximum swing $V_{OV} \leq v_O \leq V_{DD}$

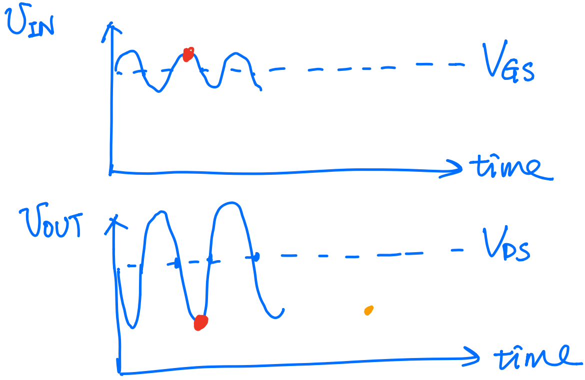


$$v_{DS,min} = V_{DS} - \underline{v_{ds}} \geq V_{GS,max} - V_{t,n}$$

$$v_{DS} - v_{ds} \geq V_{GS} + v_{gs}$$

$$v_{ds} = |A_v| v_{gs}$$

$$\boxed{v_{gs} \leq \frac{V_{DS} - V_{OV}}{1 + |A_v|}}$$



$$A_v = -k_n V_{OV} R_D$$

180° Phase shift

$|A_v| > 1$.
output amplitude larger than input.

"Easy Way" → small-signal model

$$i_D(v_{GS}, v_{DS}) = \frac{1}{2} k_n (v_{GS} - V_{t,n})^2 \underline{(1 + \lambda v_{DS})}$$

consider channel length modulation

To simplify, $\lambda = 0$

$$i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2 \quad , \quad i_D = I_D + i_d$$

$$v_{GS} = V_{GS} + v_{gs}$$

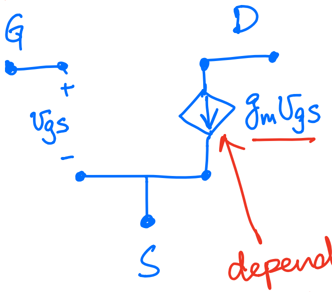
$$i_D = I_D + \underbrace{\left.\frac{\partial i_D}{\partial v_{gs}}\right|_Q}_{} \cdot v_{gs}$$

g_m

$i_D = I_D + g_m \cdot v_{gs}$ $\qquad$ $g_m = k_n(V_{GS} - V_{t,n}) = k_n V_{OV}$

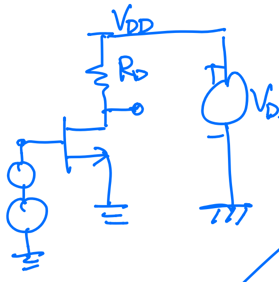
Equivalent circuit

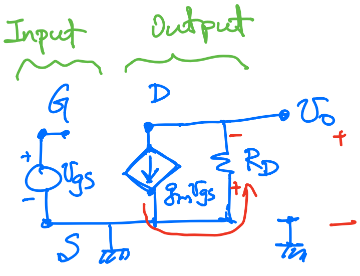
Hybrid π model



dependent current source

π





DC voltage source

→ short circuit

DC current source

→ Open

Circuit

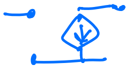
$v_o = -\underbrace{(g_m v_{gs})}_{\text{current}} \cdot R_D$

① Solve bias point, Q

V_{DS}, I_D, V_{GS}

② Find small-signal parameters

$g_m = k_n V_{OV} = k_n(\underline{V_{GS}} - V_{t,n})$ ← only dep on. DC values i.e. Q point

③ Replace  with 

Replace DC voltage source with short ckt

Replace DC current " " open ckt

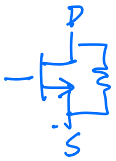
④ KCL, KVL for AC equivalent circuit

Complete model $\qquad$ $i_D = \underline{\frac{1}{2}k_n(V_{GS}+v_{gs}-V_{t,n})^2}(1+\lambda(\underline{V_{DS}}+v_{ds}))$

$$i_D = I_D + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q \cdot v_{ds}$$

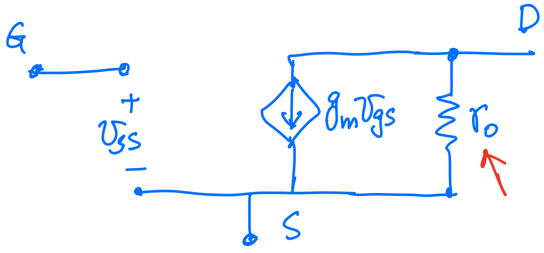
$$= I_D + g_m v_{gs} + \frac{v_{ds}}{r_o} \leftarrow \qquad r_o = \frac{1}{\lambda I_D}$$

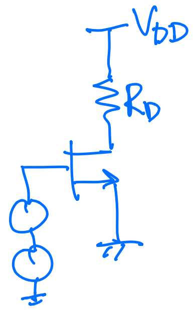
$$\frac{\partial I_D}{\partial V_{DS}} = \underset{\uparrow}{\lambda} \cdot \underbrace{\frac{1}{2} k_n (V_{GS} - V_{tn})^2}_{I_D} = \lambda I_D = \frac{1}{r_o}$$

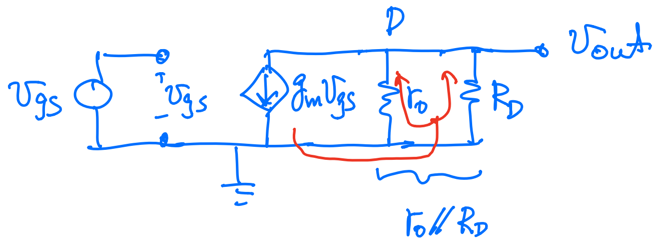


$$r_o = \frac{\Delta v_{ds}}{\Delta i_{ds}}$$

Hybrid π model







$$A_v = -g_m (r_o // R_D)$$

impact of output resistance of the MOS on overall gain