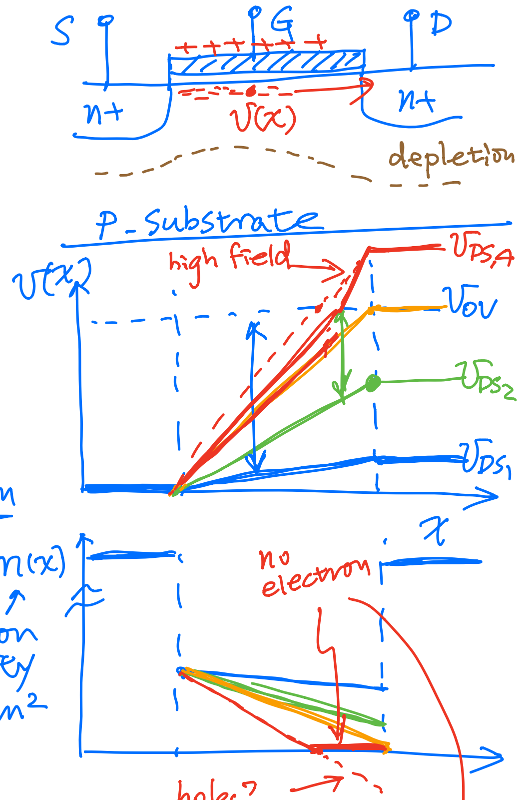
Summary

$$i_D = \underbrace{\underbrace{\mu_n C_{ox}}_{k'_n}\left(\frac{W}{L}\right)}_{k_n}\left(V_{ov}V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

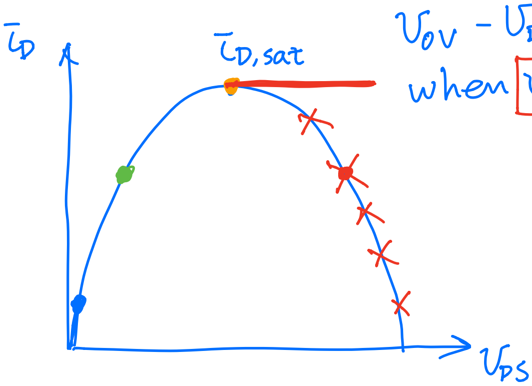


$$\frac{\partial i_D}{\partial V_{DS}} = 0$$

$$V_{ov} - V_{DS} = 0$$

when $V_{DS} = V_{ov}$

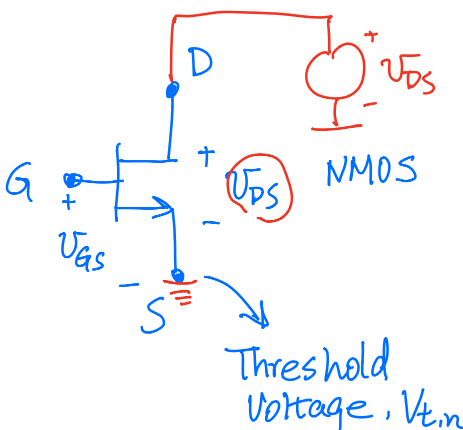
$= V_{GS} - V_{t,n}$

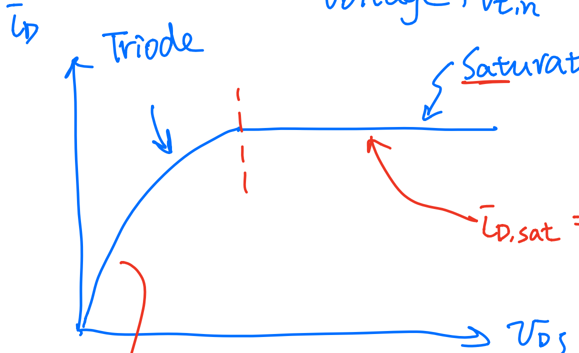


$$n(x) = C_{ox}\cdot\left(V_{GS} - v(x) - V_{t,n}\right)$$

$$= C_{ox}\left(V_{ov} - v(x)\right)$$

"pinch-off" the channel



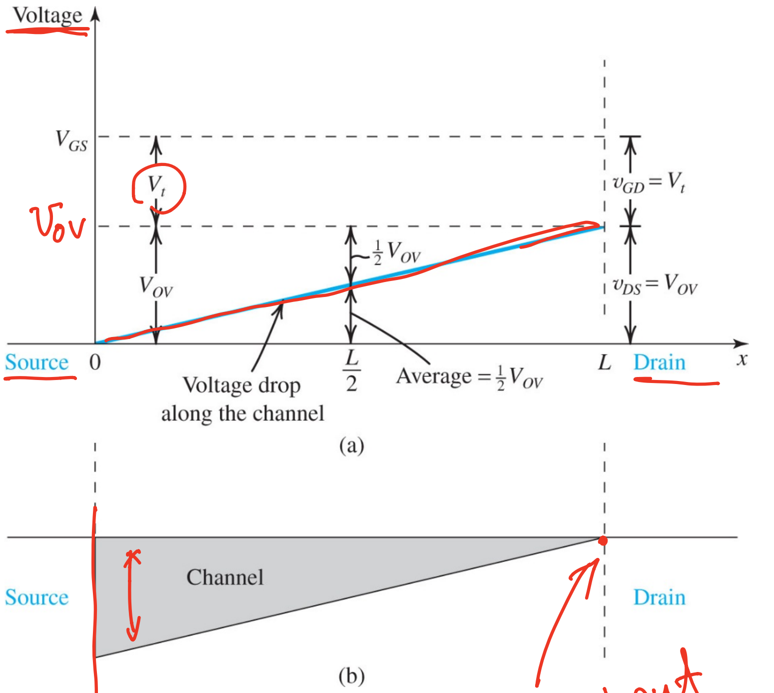


$$i_{D,sat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\cdot V_{ov}^2$$

← indep of V_{DS}

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{ov}V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

Pinch-Off



The channel potential at the drain side is v_{DS}.

When $v_{DS} = v_{OV}$, the local charge density there

$$\frac{|Q|}{\text{area}} = C_{ox}\left(v_{GS} - v_{DS} - V_t\right) = C_{ox}\left(v_{OV} - v_{DS}\right) = 0$$

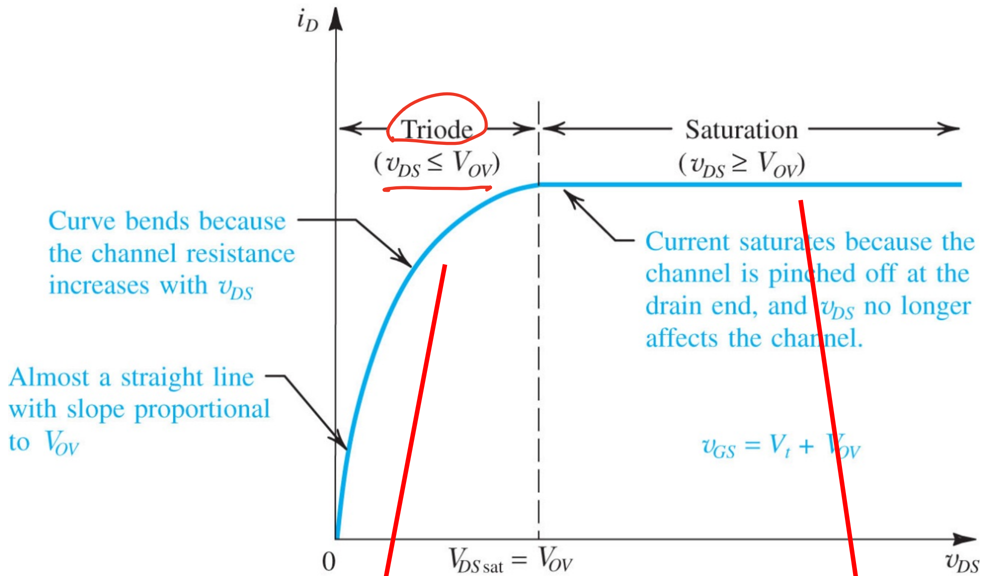
So the channel is "pinched off" near the Drain.

Once the channel is pinched off, the drain current remains constant:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

This region, $v_{DS} > v_{OV}$, is called "Saturation"

Saturation Region ($v_{DS} > v_{OV}$)



When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

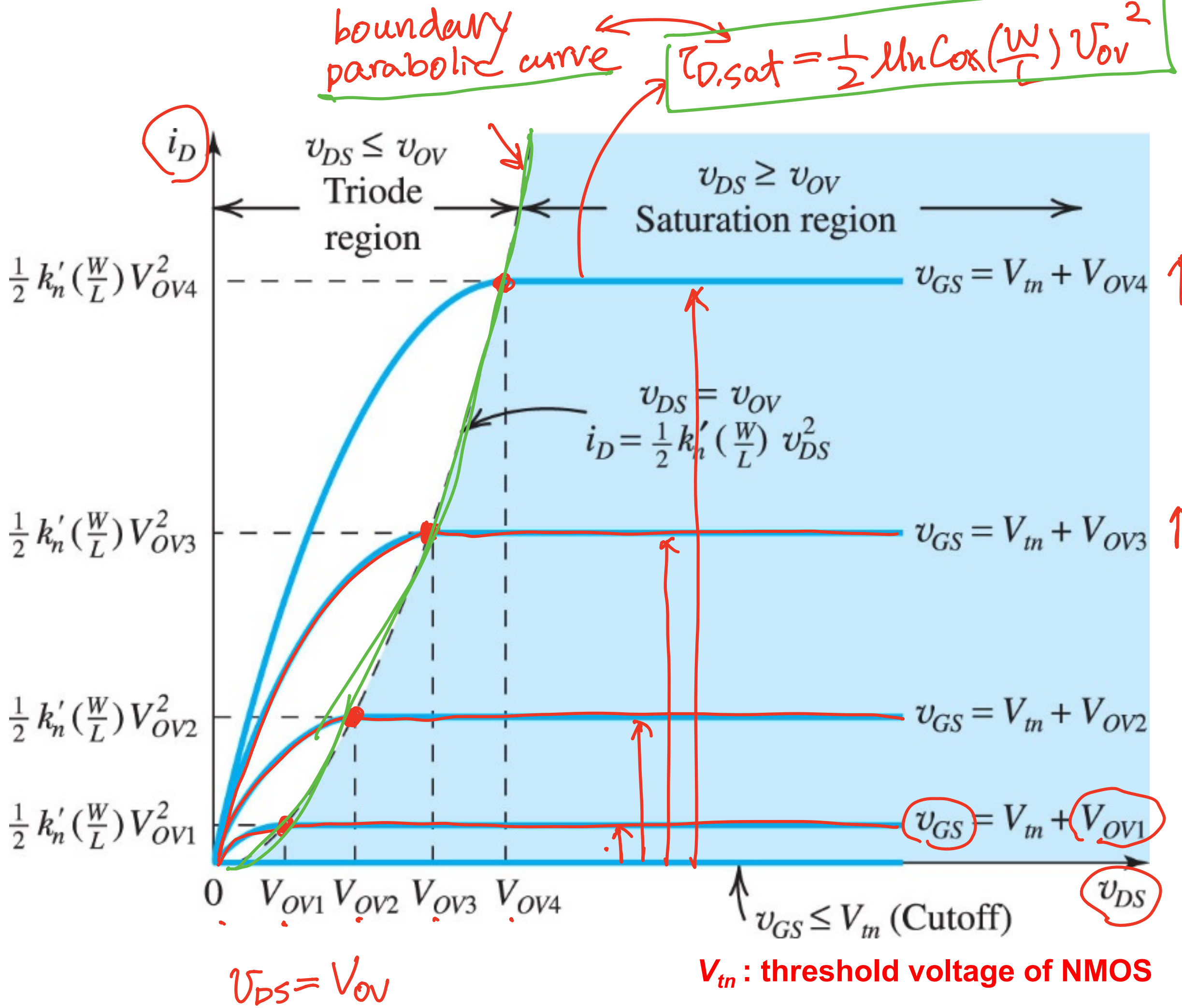
This is called the "Triode Region"

When $v_{DS} > v_{OV}$,

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2$$

This is called "Saturation Region"

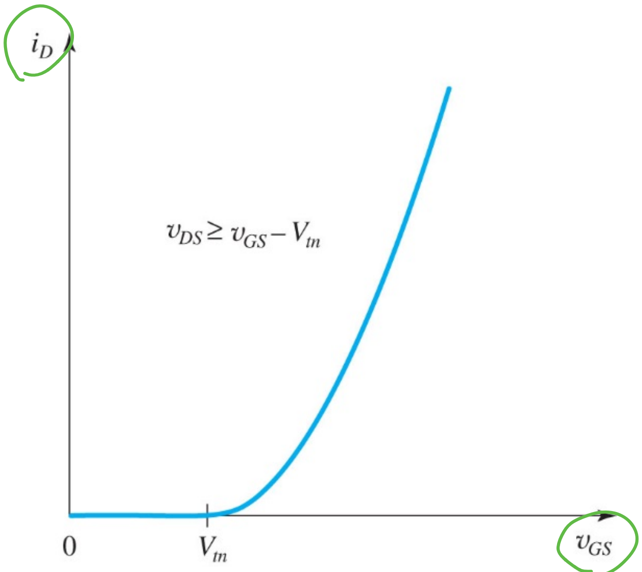
Full I-V Curves of NMOSFET



V_{tn} : threshold voltage of NMOS

Drain Current vs Gate Voltage

i_D, v_{DS}, $v_{GS} = v_{ov} + V_{t,n}$



In Saturation Region

square law

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

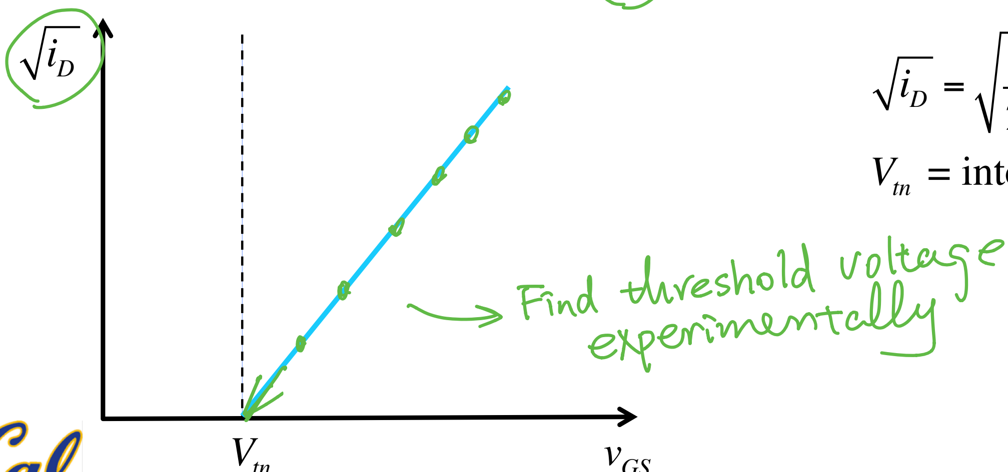
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{tn})^2$$

To experimentally determine V_{tn} :

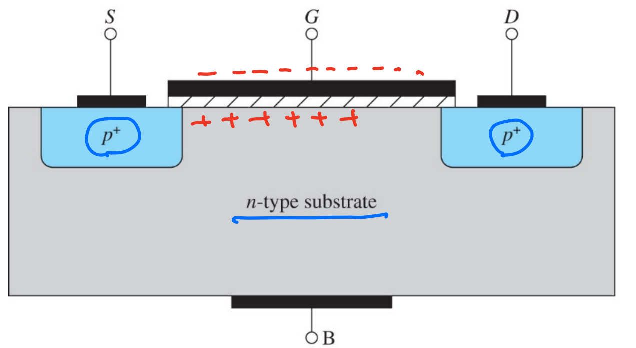
Measure and plot $\sqrt{i_D}$ versus v_{GS}

$$\sqrt{i_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}(v_{GS} - V_{tn})$$

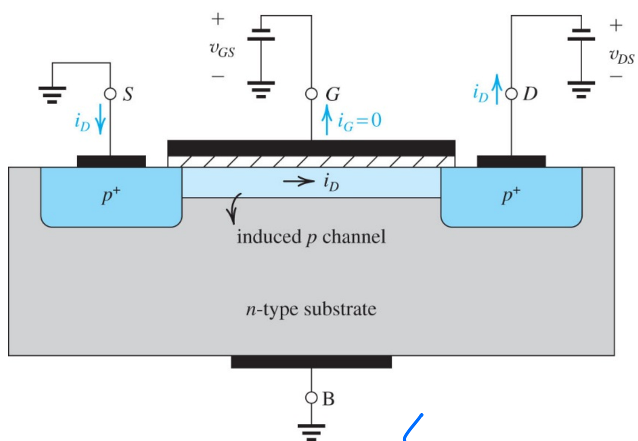
V_{tn} = intercept with horizontal axis



PMOSFET (or simply PMOS)



(a)



(b)

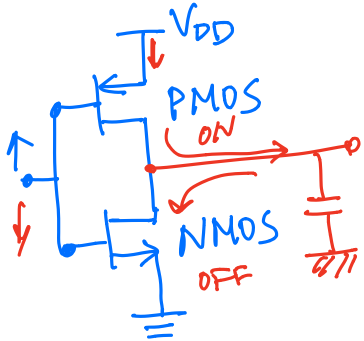
- **P-channel MOSFET**
  - **Current conducted by holes**
- **3 terminal device**
  - **Source (S): p+ (heavily p-type)**
  - **Drain (D): p+**
  - **Gate (G): metal deposited on insulator above channel**
- **Substrate (called "Body") is a 4th terminal**
  - **Substrate is n-doped**
- **Holes is induced in channel when a negative gate voltage is applied**
- **Holes moves from Source to Drain**
  - **Current flows from S to D**

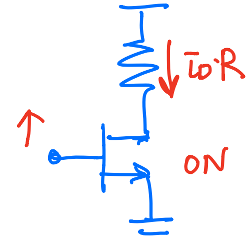
$$i_D = \mu_p C_{ox}\left(\frac{W}{L}\right)\left(|v_{ov}||v_{DS}| - \frac{1}{2}|v_{DS}|^2\right)$$

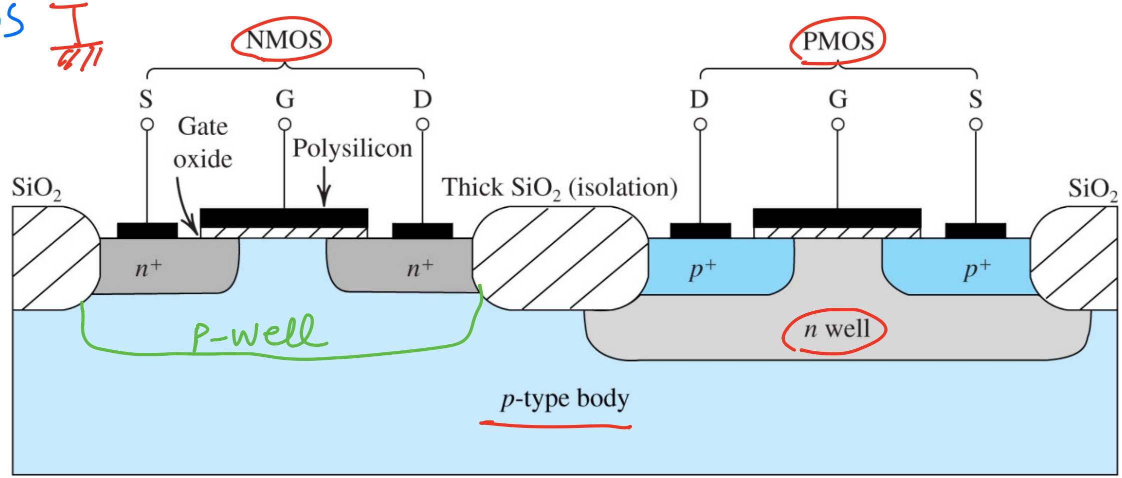
For Si $\mu_n \approx 3\mu_p$

Often use 3x width for PMOS

CMOS (Complementary MOS)







- **CMOS is the prevalent IC technology today**
- **Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a "well"**
- **PMOS is placed in an "n well" here.**
- **Alternatively, NMOS can be placed in p well**