EE105
Microelectronic Devices and Circuits:
MOSFET

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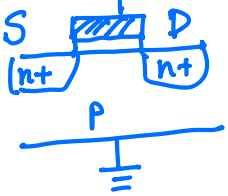
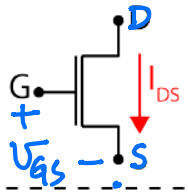


Simplest Model of MOSFET (from EE16B)

N-type MOSFET (NMOS)

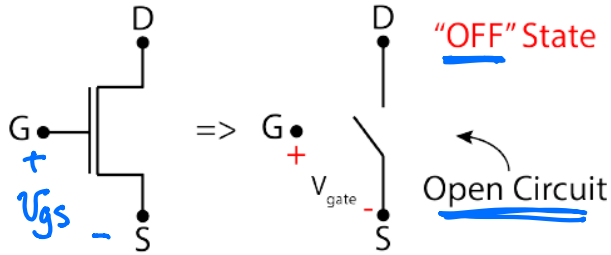


$V_{gate} = V_{GS}$

$V_{DS} > 0$

$I_{DS} > 0$

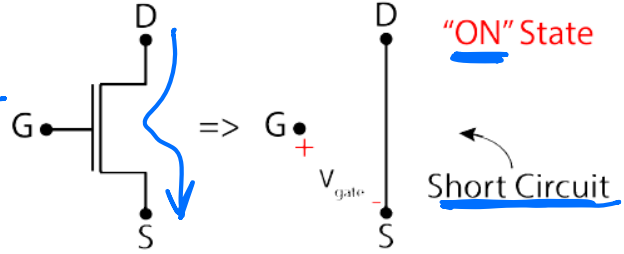
Case 1. $V_{gate} < V_{th,N}$



"OFF" State

Open Circuit

Case 2. $V_{gate} > V_{th,N}$



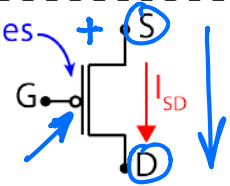
"ON" State

Short Circuit

P-type MOSFET (PMOS)

Note bubbles

V_{SG} a V_{gate}

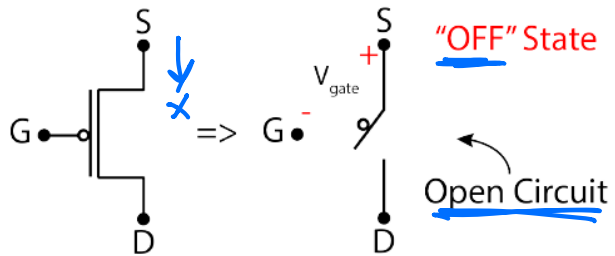


$V_{gate} = V_{SG}$

$V_{SD} > 0$

$I_{SD} > 0$

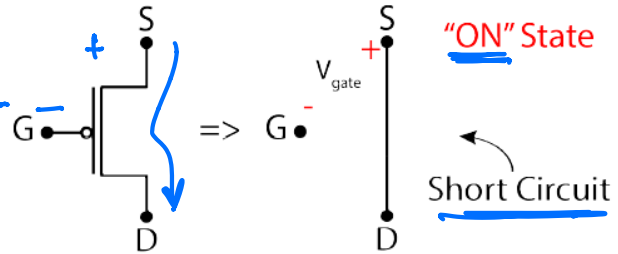
Case 1. $V_{gate} < V_{th,P}$



"OFF" State

Open Circuit

Case 2. $V_{gate} > V_{th,P}$

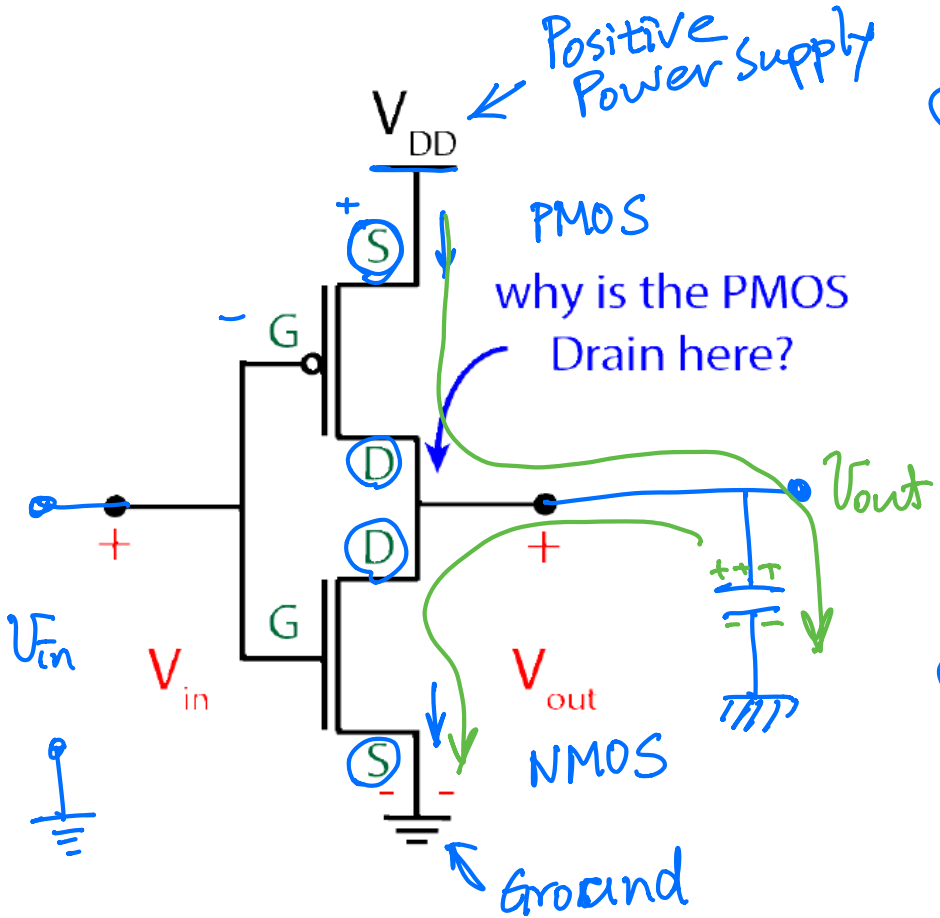


"ON" State

Short Circuit

$V_{th,n} \neq V_{th,p}$

CMOS Inverter



$V_{in} = V_{GS}$ of NMOS

① When V_{in} is high

$V_{in} = V_{DD} > V_{th,n}$

NMOS is ON

$V_{out} = 0 \rightarrow$ "Low"

$V_{SG}(PMOS) = V_{DD} - V_{DD} = 0 < V_{th,p}$

PMOS is OFF

② V_{in} is "Low"

$V_{in} = 0 = V_{GS}(NMOS) < V_{th,n}$

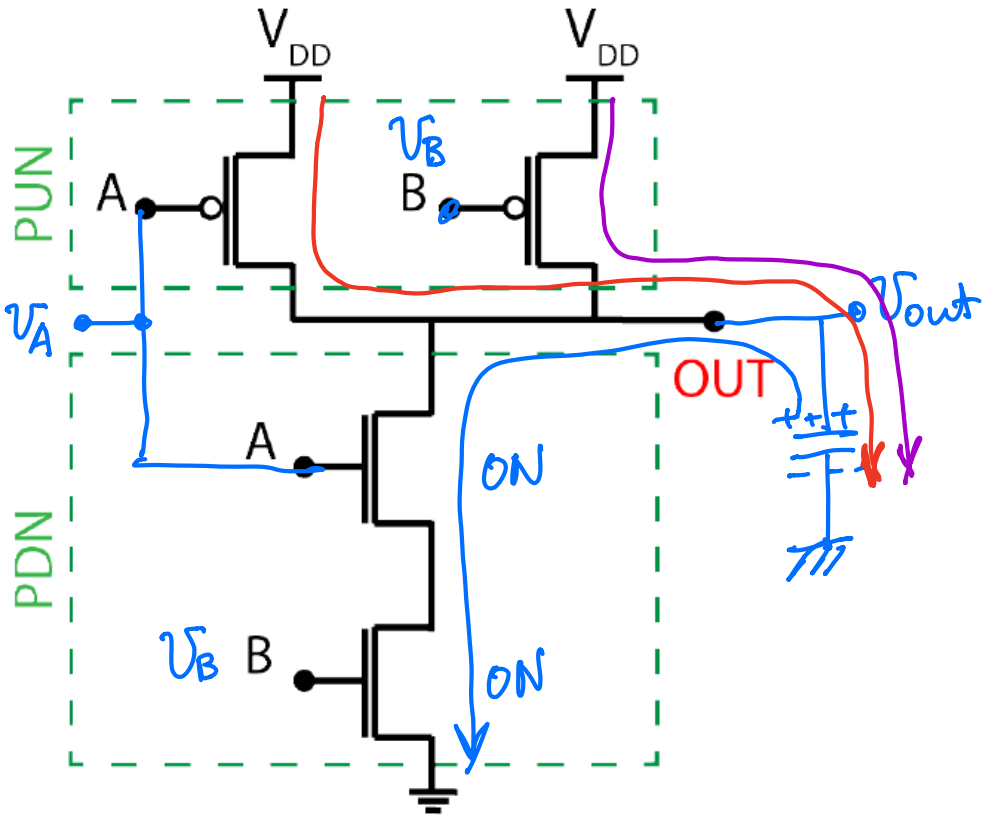
NMOS is OFF

$V_{SG} = V_{DD} - 0 = V_{DD} > V_{th,p}$

PMOS is ON

$V_{out} = V_{DD} =$ "High"

CMOS NAND Gate



A="1" , B="1"

Both NMOS's are ON

V_{out} = 0 V ⇒ "0"

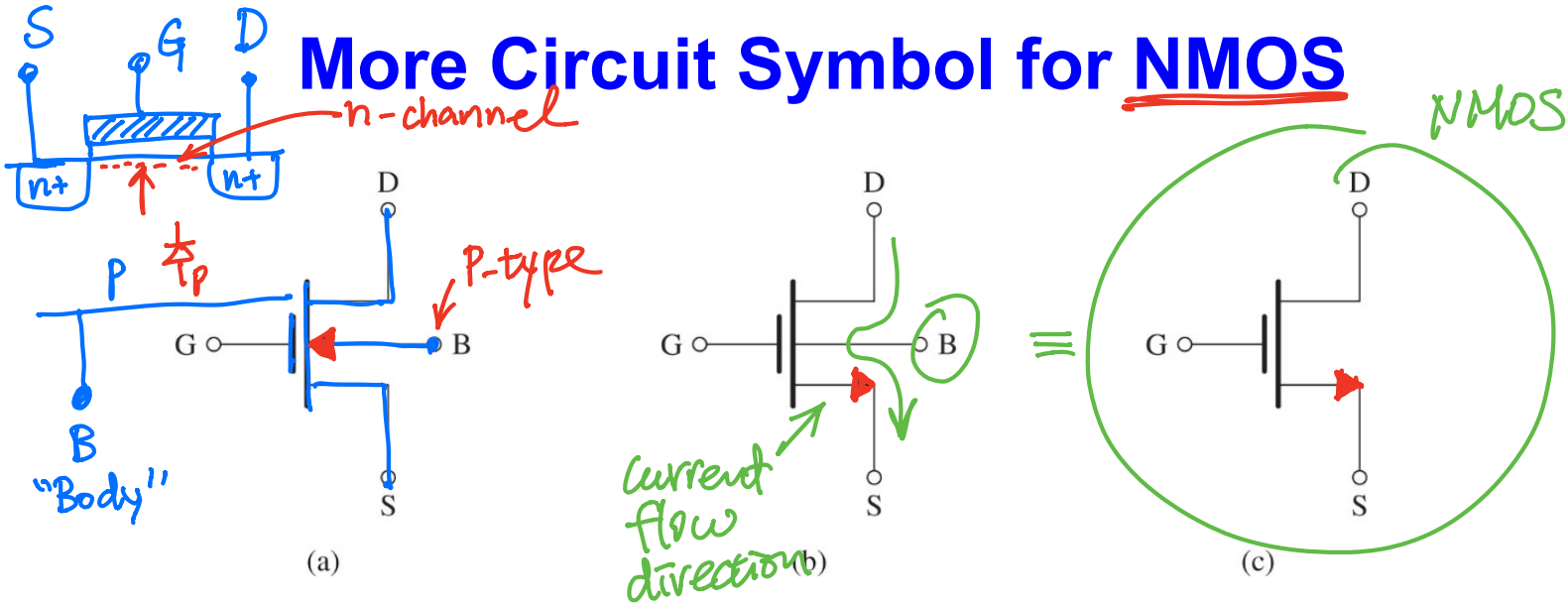
A="0" or B="0"

⇒ $V_{out} = V_{DD}$

→ "1"

A	B	out = AB
1	1	0
0	1	1
1	0	1
0	0	1

More Circuit Symbol for NMOS



4 terminal including Body (Arrow pointing to channel indicating substrate is p-type)

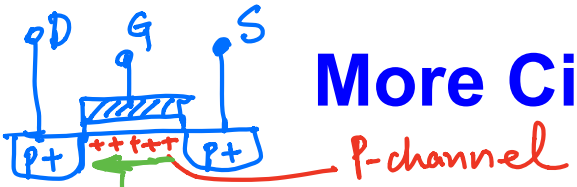
Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)

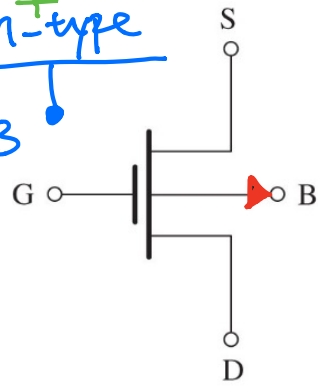
Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

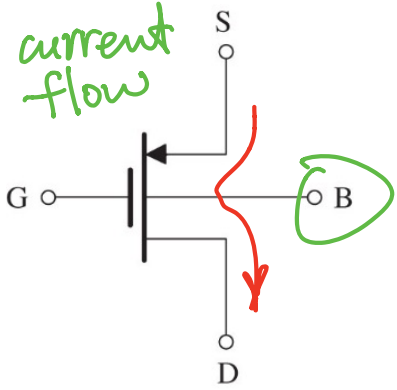
Note in NMOS

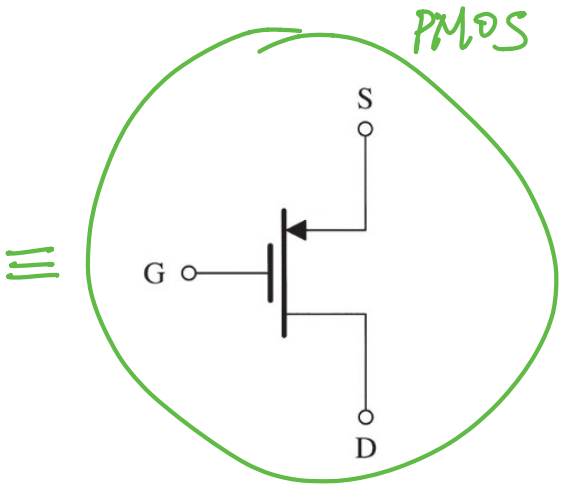
1. **Drain voltage is always more positive than Source voltage**
2. **Current always flows from Drain to Source**

More Circuit Symbol of PMOS









4 terminal including Body (Arrow pointing away from channel indicating substrate is n-type)

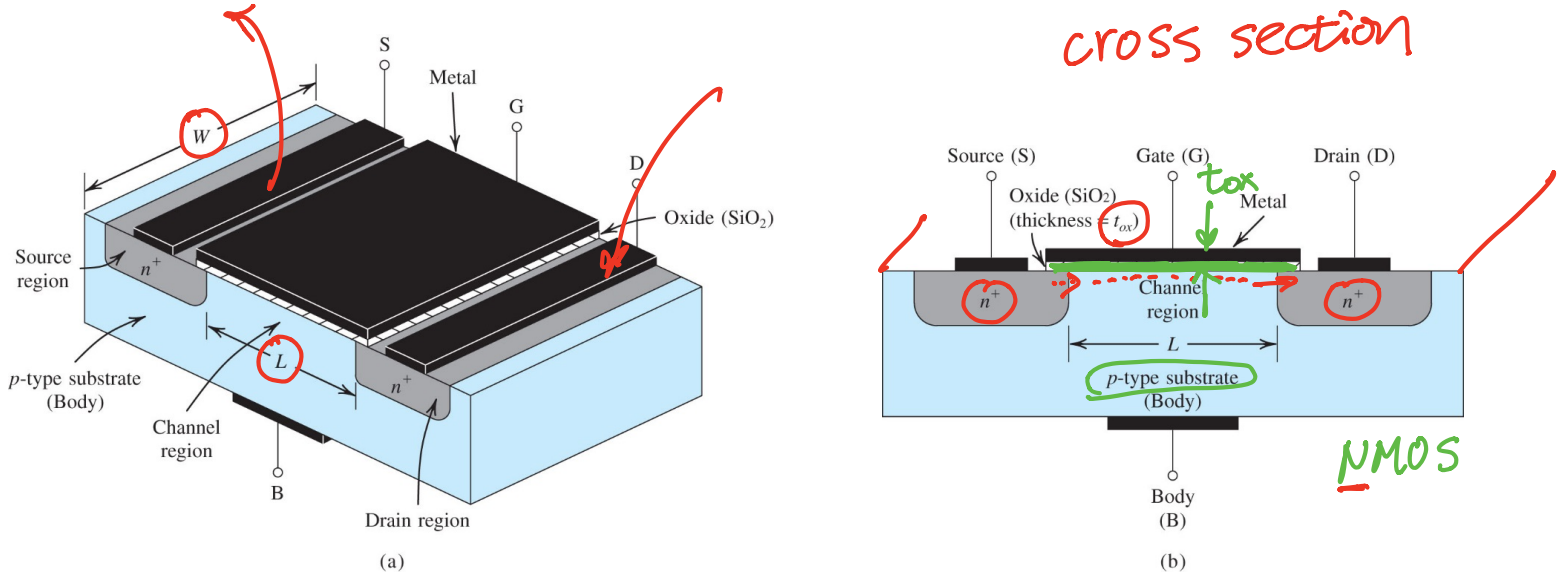
Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)

Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in PMOS

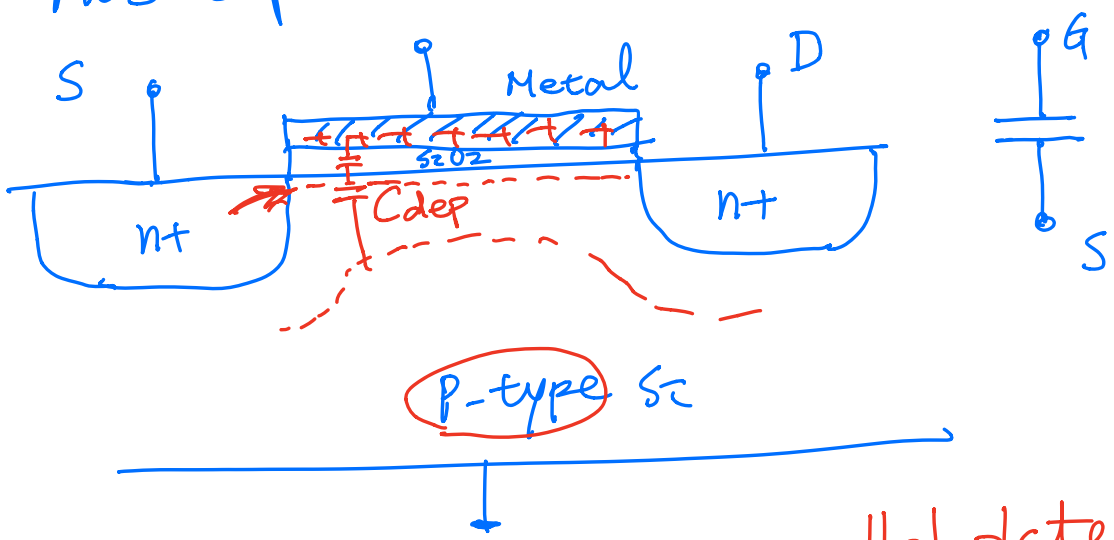
1. **Source voltage is always more positive than Drain voltage**
2. **Current always flows from Source to Drain**
3. **Source is usually drawn on top so current flows downward (convention)**

MOSFET Device Structure



- **MOSFET: metal-oxide-semiconductor field effect transistor**
- **Typically** (correlated to technology node)
  - **Channel length: L ~ < 10 nm to 0.35 μm,**
  - **Channel width: W ~ 0.05 μm to 100 μm,**
  - **Oxide thickness: t_{ox} ~ 1 to 10 nm**

MOS Capacitor



① $V_{gate} \ll 0 \Rightarrow$ MOS like parallel plate

$C = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ per unit area $\left[\frac{F}{cm^2}\right]$

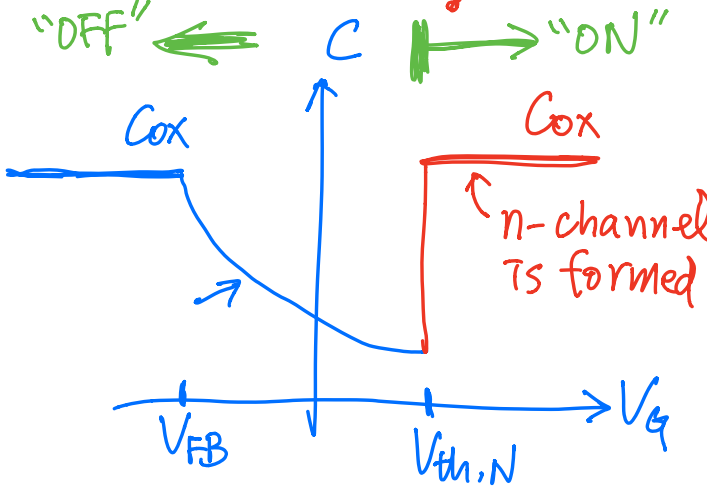
② $V_{gate} < V_{th,N}$

"like" reverse-biased p-n junction

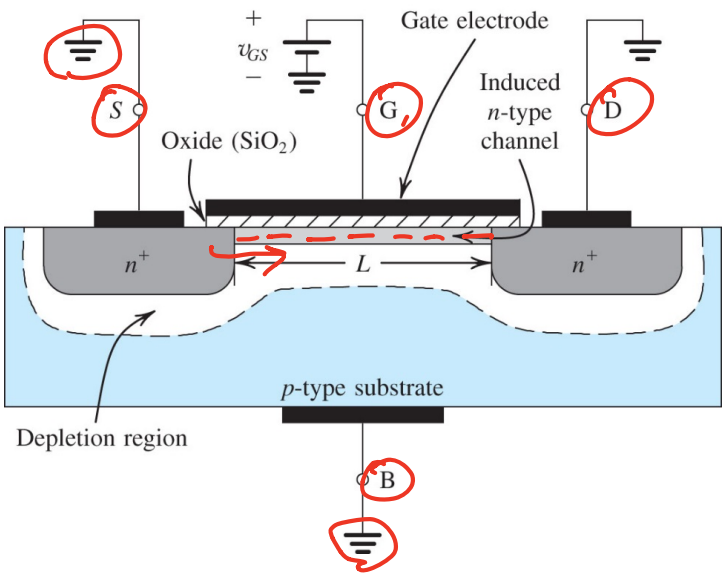
$C = \left[\frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{dep}}}\right] = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}}$

③ $V_{gate} > V_{th,N}$

$C = C_{ox}$



NMOSFET (or simply NMOS)



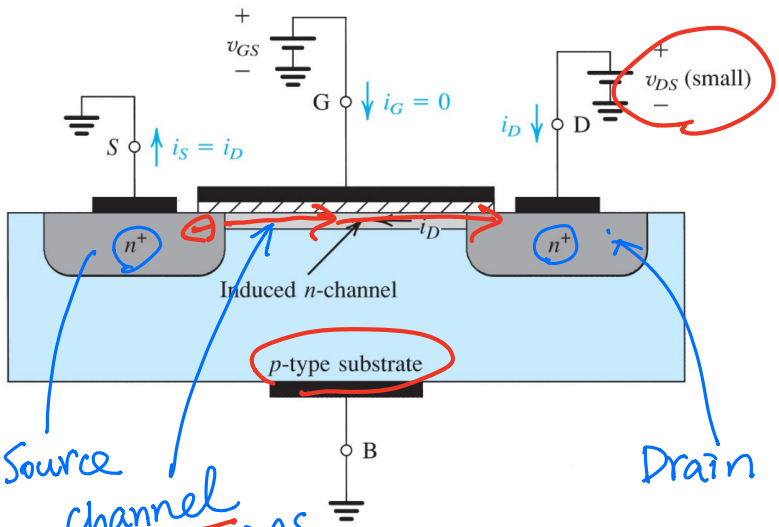
- **N-channel MOSFET**
  - **Current conducted by electrons**
- **3 terminal device**
  - **Source (S): n+ (heavily n-type)**
  - **Drain (D): n+**
  - **Gate (G): metal deposited on insulator above channel**
- **Substrate (called "Body") is a 4th terminal**
  - **Substrate is p-doped**
- **Electrons is induced in channel when a positive gate voltage is applied**
- **Electrons moves from Source to Drain**
  - **Current flows from D to S**

$V_{DS} > 0$ $I_{DS} > 0$

- current flows from D to S
- electron flows from S to D

Creating a "Channel" for Current Flow

$v_{GS} > V_t \Rightarrow$ Inversion



MOS is a capacitor across an insulator (oxide)

When a positive voltage is applied at Gate, electrons are induced under the gate.

At "thresold", sufficient number of electrons form a "channel" between Source and Drain, forming a conductive channel.

Total charge in the channel:

$$|Q| = C_{ox} \cdot WL \cdot (v_{GS} - V_t)$$

where $C_{ox} = \dfrac{\varepsilon_{ox}}{t_{ox}}$ is oxide capacitance per unit area

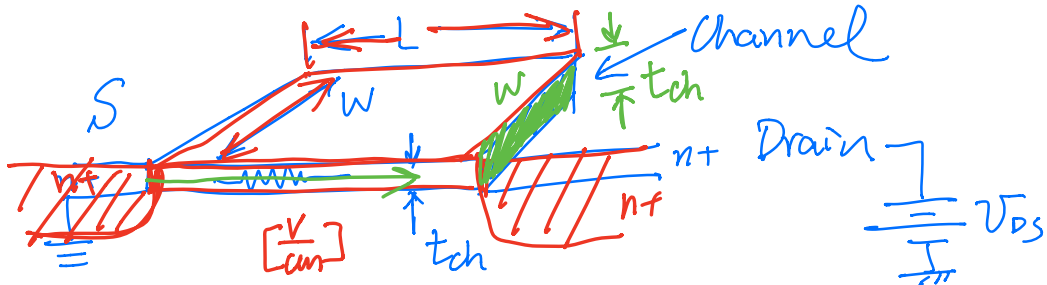
$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12}$ F/m

W : gate width

L : gate length

V_t : Threshold voltage

$v_{GS} - V_t \equiv v_{OV}$ is called "Overdrive Voltage"



$$J = \sigma \cdot E = (n q \mu_n)\left(\frac{V_{DS}}{L}\right) \qquad E = \frac{V_{DS}}{L}$$

$\left[\frac{A}{cm^2}\right]$ conductivity n: $\frac{V_{DS}}{L}$

$Q = C \cdot \Delta V$

MOS capacitor

$V_{th,n}$

$$Q = CV = C_{ox}(V_{GS} - V_t) \cdot W \cdot L$$

Coul $\left[\frac{F}{cm^2}\right][V]$ per unit area area $[cm^2]$

$$\left[\frac{1}{cm^3}\right][coul]\, n q = \frac{Q}{W \cdot L \cdot t_{ch}} \qquad \left[\frac{coul}{cm^3}\right]$$

$$I_{DS} = J \times t_{ch} \cdot W \quad \leftarrow \text{area of channel}$$

$$= \underbrace{n q \mu_n \left(\frac{V_{DS}}{L}\right)}_{\sigma} \underbrace{t_{ch} \cdot W}_{E}$$

$$= \underbrace{\frac{C_{ox}(V_{GS} - V_t) \cdot W \cdot L}{W \cdot L \cdot t_{ch}}}_{n} \cdot \mu_n \cdot t_{ch} \cdot W \left(\frac{V_{DS}}{L}\right)_{E}$$

$I_{DS} \propto V_{DS}$

$$I_{DS} = \mu_n C_{ox} (V_{GS} - V_t)\left(\frac{W}{L}\right) \cdot V_{DS}$$

"Aspect ratio"

Equivalent resistance

$$R_{ch} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_n C_{ox}(V_{GS} - V_t) \cdot \left(\frac{W}{L}\right)}$$

gate bias; Geometry

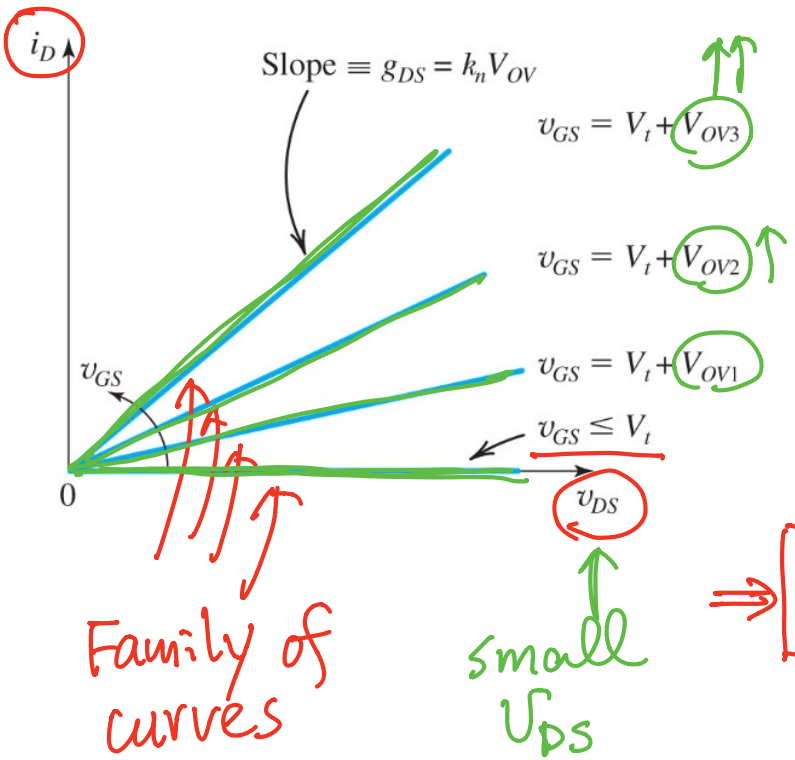
Large-Signal Model

(usually used to solve DC bias voltage and current)

Current at Small v_{DS}

3-terminal D.S.G

i_{DS} (current from D to S)



When $v_{OV} = v_{GS} - V_t > 0$, a channel is formed between Source and Drain.

Linear charge density in channel:

$$\frac{|Q|}{L} = C_{ox} W \cdot v_{OV}$$

Electric field along the channel

$$|E| = \frac{v_{DS}}{L}$$

Drain current = charge density x velocity:

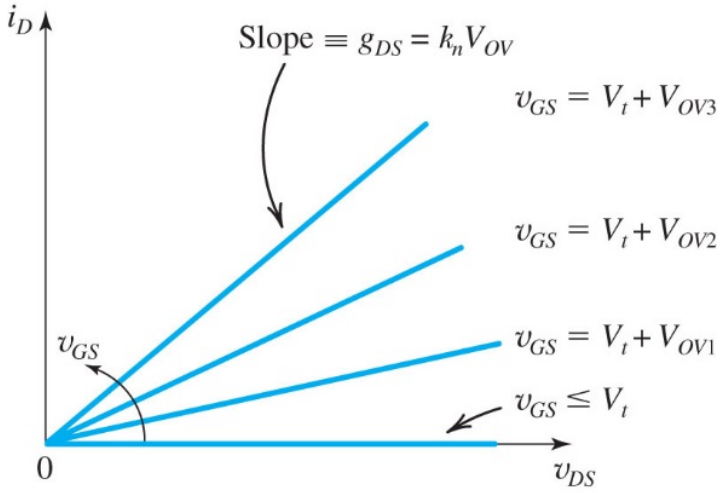
$$i_D = \frac{|Q|}{L} v_n = \frac{|Q|}{L} \mu_n |E| = C_{ox} W \cdot v_{OV} \mu_n \frac{v_{DS}}{L}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

$v_{GS} - V_{t,n}$

At small v_{DS}, the transistor is like a gate-controlled variable resistor

Current at Small v_{DS}



$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

$$= k_n' \frac{W}{L} v_{OV} v_{DS}$$

$$= k_n v_{OV} v_{DS}$$

where

$k_n' = \mu_n C_{ox}$: process transconducance paramter

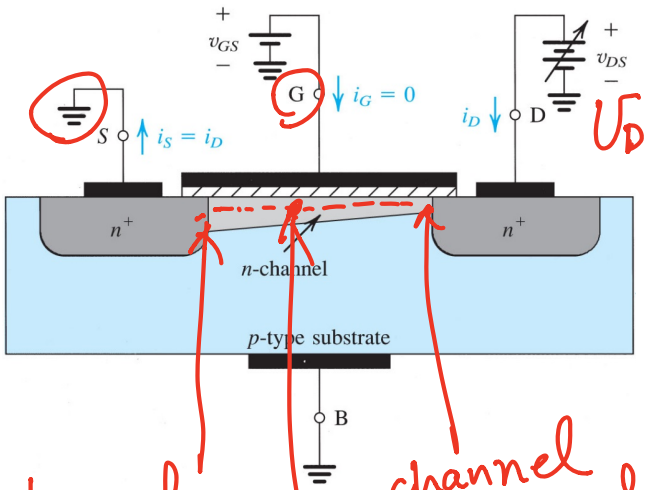
$k_n = \mu_n C_{ox} \left(\frac{W}{L}\right)$: MOSFET transconductance parameter

MOSFET behaves like a linear resistor

$$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{k_n v_{OV}}$$

Resistance value can be changed by gate voltage (overdrive voltage)

Triode Region ($v_{DS} < v_{OV}$)



channel potential = 0, $x = 0$

$v(x)$

channel potential = v_{DS}, $x = L$

$v(x=0) = 0$

$v(L) = v_{DS}$

$Q(x) = C_{ox}(v_{GS} - v(x) - V_{t,n})$

voltage drop across channel

As v_{DS} increases, the potential in the channel is no longer a constant. Assume the channel is $v(x)$:

$$i_D = C_{ox} W \left(v_{GS} - v(x) - V_t\right) v_n(x)$$

$$v_n(x) = \mu_n \left|E(x)\right| = \mu_n \frac{dv(x)}{dx}$$

Note: i_D is still constant along the channel (think Kirchhoff's Current Law)

Integrate along the channel

$$\int_{x=0}^{x=L} i_D dx = \int_{x=0}^{x=L} \left(C_{ox} W \left(v_{GS} - v(x) - V_t\right) \mu_n \frac{dv(x)}{dx}\right) dx$$

Change of variable on right-hand side: $x \rightarrow v$

$$i_D L = \int_{v=0}^{v=v_{DS}} \left(C_{ox} W \left(v_{OV} - v\right) \mu_n\right) dv$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

$$\bar{I}_D = \bar{I}_{DS} = \mu_n C_{ox} \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{tn}) \cdot V_{DS}$$

small V_{DS}
E field constant

$$\Downarrow$$

$V_{GS} - V(x) - V_{tn}$

↑ channel potential

$$\downarrow$$

$$E = \frac{V_{DS}}{L}$$

$$\bar{I}_D = \mu_n C_{ox} W \left(V_{GS} - V(x) - V_{tn}\right) \frac{dV(x)}{dx}$$

$\bar{I}_D$: constant for a given V_{DS}
Want $\bar{I}_{DS}$, V_{DS}

$\frac{dV(x)}{dx} = E(x)$
Not assume E is constant

KCL, $\bar{I}_D$ = constant

$$\int_0^L \bar{I}_D \cdot dx = \bar{I}_D \cdot L = \mu_n C_{ox} W \int_0^L \left(V_{GS} - V(x) - V_{tn}\right) \frac{dV}{dx} dx$$

$V(L) = V_{DS}$
$V_{OV} = V_{GS} - V_{tn}$

$$= \mu_n C_{ox} W \int_0^{V(L)=V_{DS}} (V_{OV} - V) \cdot dV$$

$$= \mu_n C_{ox} W \left[V_{OV} \cdot V_{DS} - \frac{1}{2} V^2 \Big|_0^{V_{DS}} \right]$$

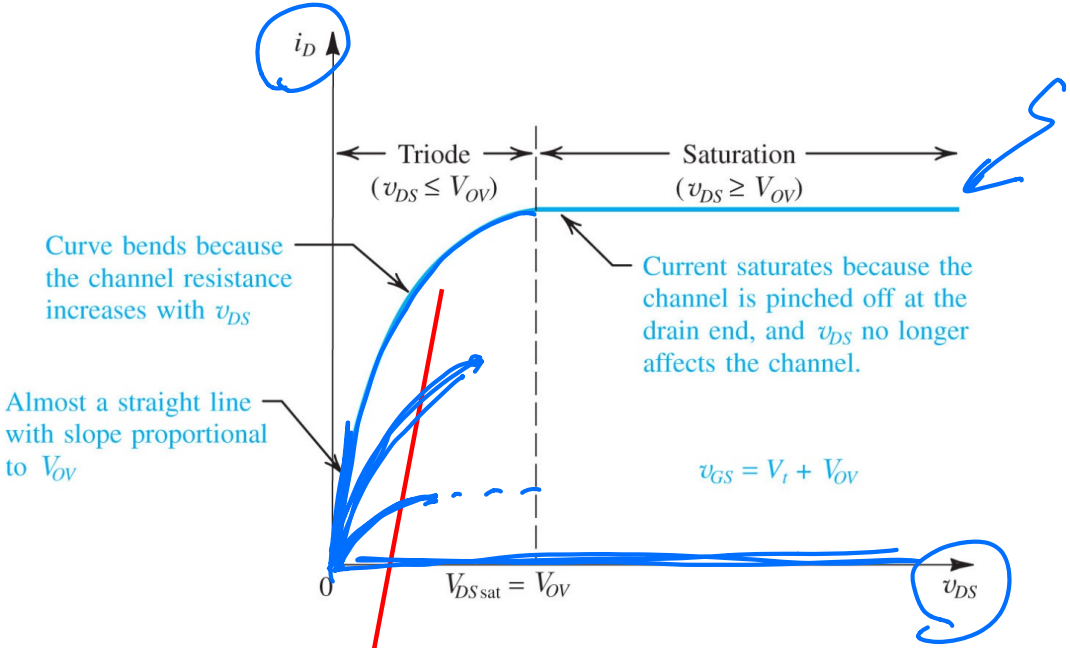
$$= \mu_n C_{ox} \cdot W \left[V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Check $V_{DS} \ll V_{OV}$ same expression

$$\bar{I}_D \rightarrow \mu_n C_{ox} \frac{W}{L} \cdot V_{OV} \cdot V_{DS}$$

$$\bar{I}_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left(V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

Triode Region ($v_{DS} < v_{OV}$)

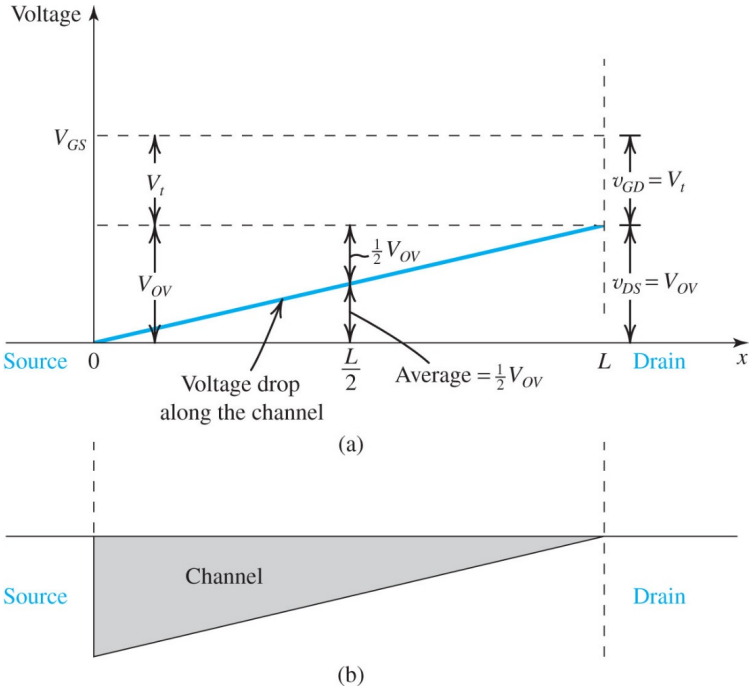


When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

This is called the "Triode Region"

Pinch-Off



The channel potential at the drain side is v_{DS}.

When $v_{DS} = v_{OV}$, the local charge density there

$$\frac{|Q|}{\text{area}} = C_{ox}\left(v_{GS} - v_{DS} - V_t\right) = C_{ox}\left(v_{OV} - v_{DS}\right) = 0$$

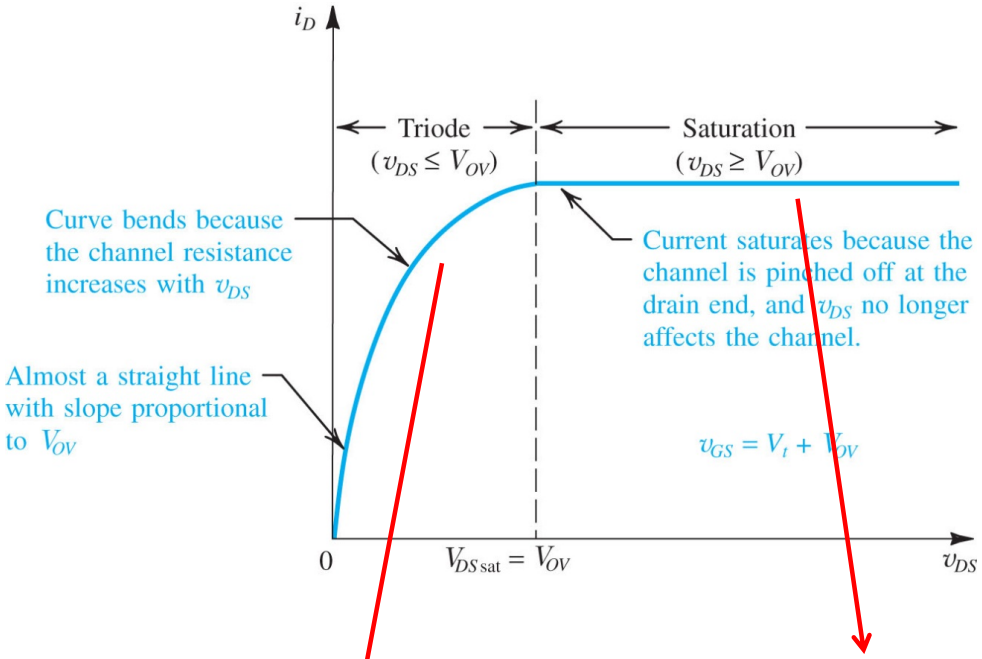
So the channel is "pinched off" near the Drain.

Once the channel is pinched off, the drain current remains constant:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

This region, $v_{DS} > v_{OV}$, is called "Saturation"

Saturation Region ($v_{DS} > v_{OV}$)



When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

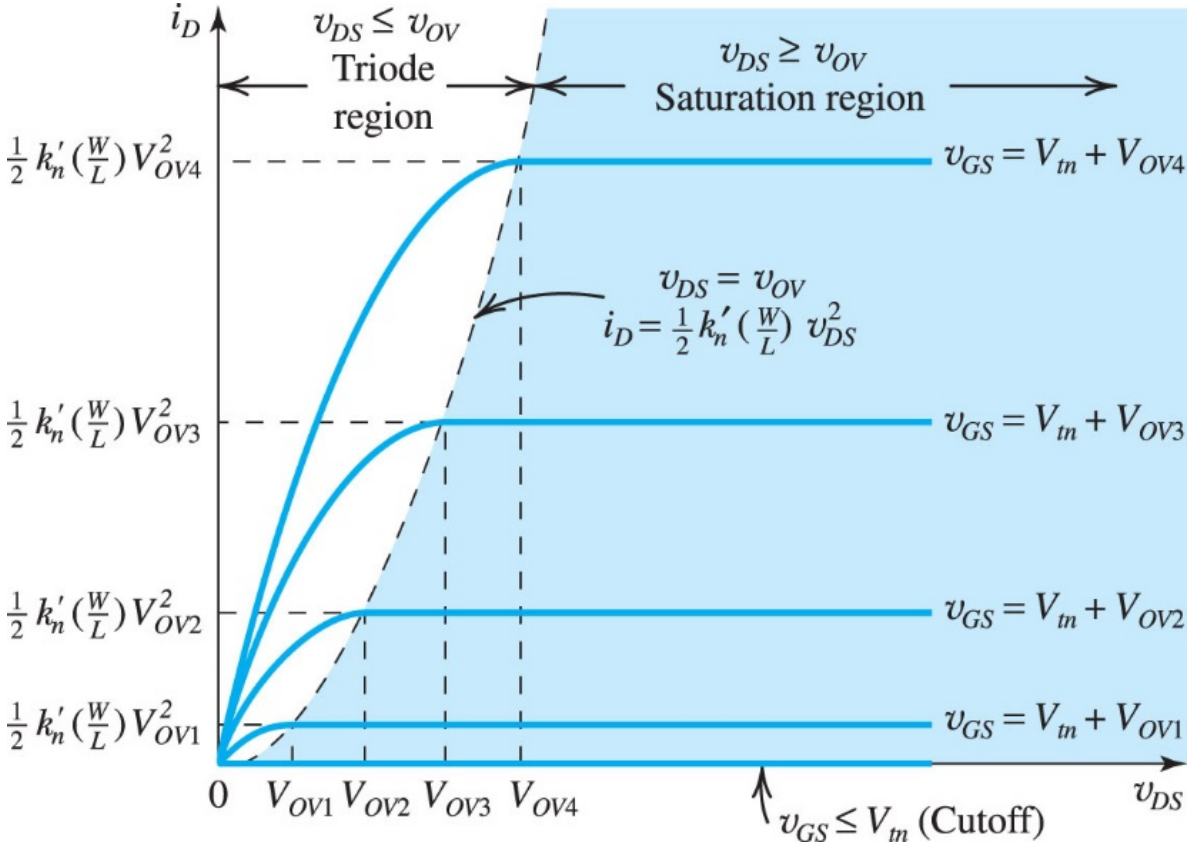
This is called the "Triode Region"

When $v_{DS} > v_{OV}$,

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2$$

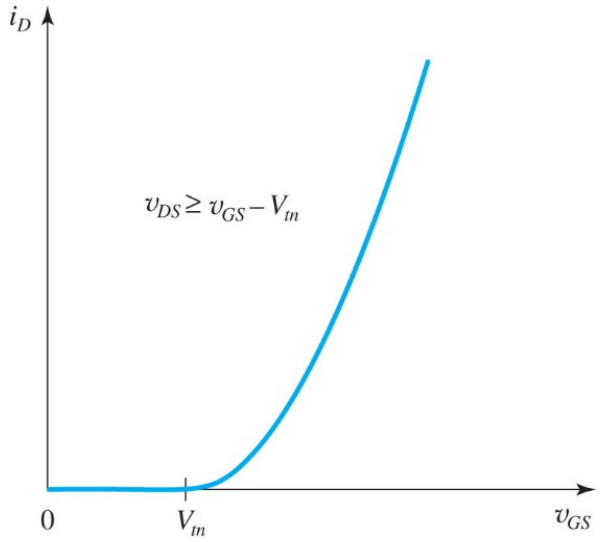
This is called "Saturation Region"

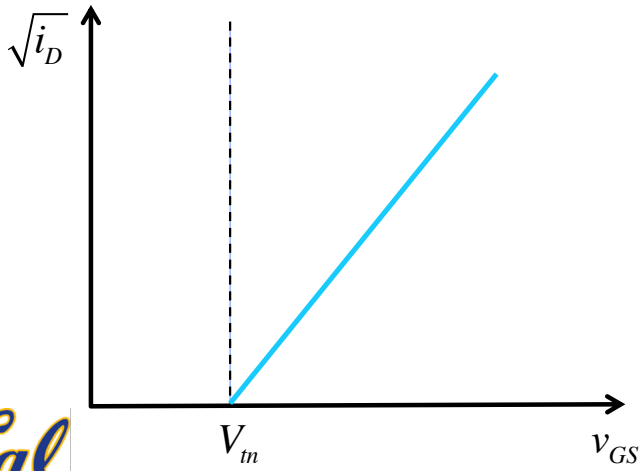
Full I-V Curves of NMOSFET



V_{tn} : threshold voltage of NMOS

Drain Current vs Gate Voltage





In Saturation Region

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v_{GS} - V_{tn}\right)^2$$

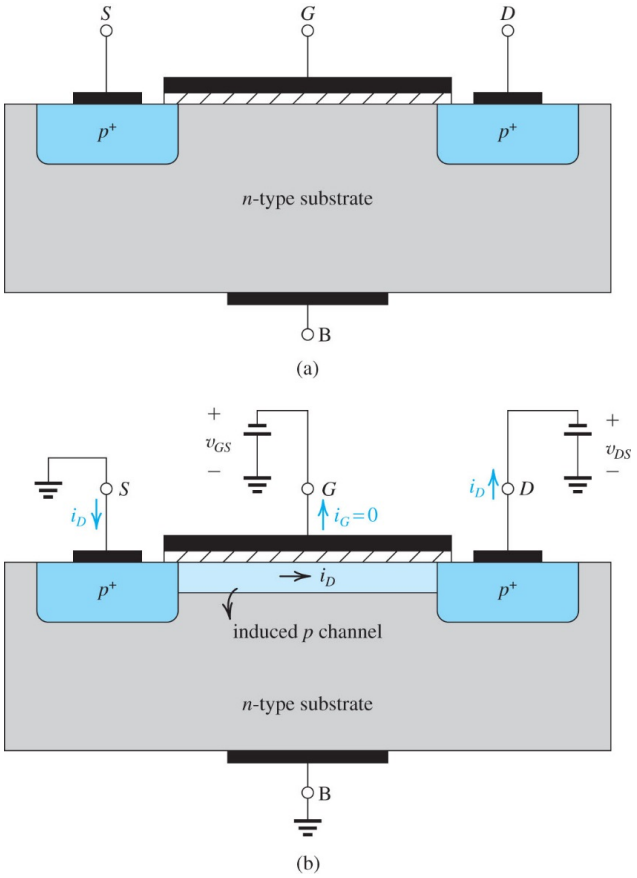
To experimentally determine V_{tn} :

Measure and plot $\sqrt{i_D}$ versus v_{GS}

$$\sqrt{i_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}\left(v_{GS} - V_{tn}\right)$$

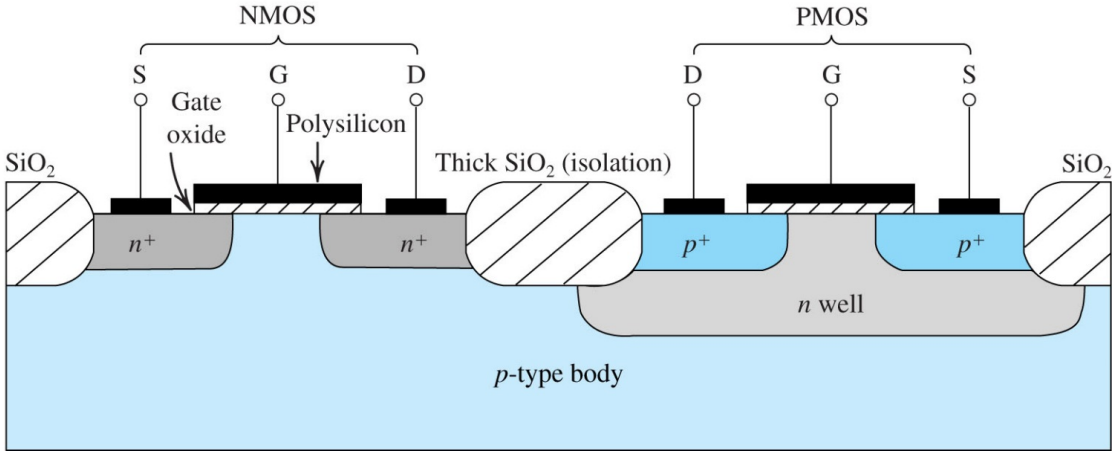
V_{tn} = intercept with horizontal axis

PMOSFET (or simply PMOS)



- **P-channel MOSFET**
  - **Current conducted by holes**
- **3 terminal device**
  - **Source (S): p+ (heavily p-type)**
  - **Drain (D): p+**
  - **Gate (G): metal deposited on insulator above channel**
- **Substrate (called "Body") is a 4th terminal**
  - **Substrate is n-doped**
- **Holes is induced in channel when a negative gate voltage is applied**
- **Holes moves from Source to Drain**
  - **Current flows from S to D**

CMOS
(Complementary MOS)



- **CMOS is the prevalent IC technology today**
- **Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a "well"**
- **PMOS is placed in an "n well" here.**
- **Alternatively, NMOS can be placed in p well**