### UNIVERSITY OF CALIFORNIA AT BERKELEY

# College of Engineering Department of Electrical Engineering and Computer Sciences

## EE105 Lab Experiments

# Lab 6: Differential Amplifier Pre-Lab Worksheet

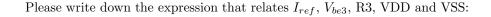
1 Pre-Lab
1.1 Differential Input Stage
Please draw the equivalent "half circuit" for the differential signals.
Please write down the expression of the differential voltage gain $(A_{dm} = (V_{o1} - V_{o2})/V_{dm})$ :
Please write down the expression of differential gain high cutoff frequency $(f_{H_{dm}})$ :
Please write down the expression of maximum differential output swing and express it in terms of DC base voltage $V_b$ :
For hand calculation only:
Resistor load R1 and R2:

### 1.2 Widlar Current Source

Tail Current Source  $I_{bias}$ :

Please write down the expression that relates  $I_{ref},\,I_{bias},\,V_t$  and R4:

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Please write down the output impedance of current mirror  $(R_{out})$ :

Please write down the expression of the minimum allowable voltage on the collector of Q4:

According to the  $I_{bias}$  from previous section, select proper R3 and R4:

Verify the performance of the current source by Hspice simulation:

Design Parameter	Hand Calculation	HSPICE Simulation
$I_{bias}$		
$I_{ref}$		
$R_{out}$		

Table 1: Widlar Current Source Design

## 1.3 Common Mode Characterization

Please draw the equivalent "half circuit" for common mode signal.

Please write down the expression of the common mode gain with 0.1% load resistor mismatch  $(A_{cm} = (V_{o1} - V_{o2})/V_{dm})$ :

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The expression of minimal common input voltage:	
The expression of maximum common input voltage:	

### 1.4 Putting it all together

Now connect the current source and differential pair together and verify its performance in Hspice

Performance	Hand Calculation	HSPICE Simulation
Differential Mode Gain $(A_{dm})$		
Differential Mode Gain High Cutoff Frequency $(f_H)$		
Differential Output Swing (SW)		
Common Mode Gain $(A_{cm})$ with mismatch		
Common Mode rejection Ratio (CMRR) with mismatch		

**Table 2:** Overall performance verification

Attach the plot of transient waveform of  $(V_{o1} - V_{o2})$  v.s.  $V_{dm}$  at a frequency below the cutoff frequency.

Attach the plot showing evidence of a 2V differential output swing.

Attach the plot of the frequency response of  $A_{dm}$  from 10Hz to 100kHz.

Attach the plot of transient waveform of  $(V_{o1}-V_{o2})$  v.s.  $V_{cm}$  with 0.1% load resistor mismatch.

Attach the plot of the frequency response of  $A_{cm}$  with 0.1% load resistor mismatch from 10Hz to 100kHz.