EECS105 Name_____
Final
5/8/12 SID_____

1,2	/30
3,4	/25
5,6	/30
7	/25
8	/30
9	/30
10	/20
11	/30
12	/30
13	/30
Total	/280

NO CALCULATORS – This is a hint. If you feel like you need to use a calculator, you're probably doing the problem wrong!

1. One half of a silicon sample is doped with 10^{20} phosphorous atoms and the other half is doped with 10^{18} boron atoms.

a. Will the depletion region be mostly in the N side or the P side?

[2] P side

b. In forward bias, will the current be mostly holes, or mostly electrons?

[2] electrons

c. In forward bias, will those carriers mostly flow from N to P, or from P to N?

[2] N to P

d. In reverse bias, which carriers, starting from which side, will form the majority of the reverse leakage current?

[4] electrons on P side

2. In a typical NPN transistor operated in the **forward active** region,

a. Is the base/emitter junction forward or reverse biased?

[3] forward

b. The base/collector junction is forward or reverse biased?

[2] reverse

c. The current flowing in the base region is primarily made up of what type of charge carriers, holes or electrons, coming from where and going where?

[6] electrons from emitter to collector

d. Is the current in part c a drift current or diffusion current?

[3] diffusion

e. The base current I_B is primarily made up of holes. What are the two components of that current (i.e. where do the holes go)?

[6] diffusion to emitter
recombination w/ electrons from emitter

3. In an NMOS device in **saturation**,

a. the current in the channel region is primarily made up of what type of carrier, holes or electrons?

[3] electrons

b. Is that current due to drift, or diffusion?

[3] drift

c. Is the drain/bulk junction forward or reverse biased?

[3] reverse

4. You have built a single-pole common source amplifier with a DC gain of -100. You measure the response at 10kHz and find that the magnitude of the gain is 10. The transistor is biased such that g_m=1mS.

a. What is the unity gain frequency?

b. What is the pole frequency?

c. What is the low frequency output impedance?

d. What is the output capacitance?

ω answers in Hz OK

R_{out}, C_{out} calculations in Hz −1 each

ω_u $2\pi \cdot 100k \frac{rad}{sec}$	ω_p $2\pi \cdot 1k \frac{rad}{sec}$	R_{out} $200\pi\ \Omega$ $628\ \Omega$	C_{out} $2\pi\ \mu F$

100kΩ

$\frac{1}{RC} = \omega_p = 2\pi \cdot 1^k$

$C = \frac{1}{100^k \cdot 2\pi \cdot 1^k} = \frac{1}{2\pi} \cdot 10^{-8} = \frac{10}{2\pi}\ nF \doteq 1.3\ nF$ ✓

[4 pts] each

5. What is the minimum current consumption of a bipolar amplifier which achieves a gain of 4 at 10^6 rad/sec while driving a 1pF load? Hint: find wu, then gm.

ω_u $4 \times 10^6 \frac{rad}{sec}$	g_m $4 \times 10^{-6} S$	I_{min} $100 nA$

[5 each]

$g_m = \omega_u C_L$ $I_{min} = g_m V_T$

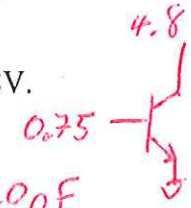
6. You have a single-pole amplifier with a DC gain of -10 and a pole at 1Grad/sec. You apply an input of $\sin(10^6 t)+\sin(10^9 t)+\sin(10^{10} t)$. Write down the output that you expect to see.

[15] 1 sign, 2 mag, 2 phase } each term

$-10\sin(10^6 t) + -7\sin(10^9 t - \frac{\pi}{4}) - \sin(10^{10} t - \frac{\pi}{2})$

$10\sin(10^6 t \pm \pi) + 7\sin(10^9 t + \frac{3\pi}{4}) + \sin(10^{10} t + \frac{\pi}{2})$

7. You have an NPN BJT with a zero-bias base/collector capacitance of C_{jc0}=1pF and a zero-bias base/emitter capacitance of C_{je0}=10pF. The built-in voltage for the base/collector junction is 0.8V, and for the base/emitter junction it's 1V. The transistor is used in a common-emitter amplifier with the V_{BE}= 0.75V and V_{CE}=4.8V. The emitter is grounded. The DC gain is -100, and the amplifier is driving a large capacitive load.



a. Estimate C_μ and C_π.

$C_\pi = \frac{10p}{\sqrt{1 - \frac{0.75}{1}}} \doteq \frac{10}{\sqrt{\frac{1}{4}}} = 20pF$

[10] $C_\mu = \frac{1pF}{\sqrt{1 - \frac{-4.05}{0.8}}} = \frac{1p}{\sqrt{6}} \approx 0.4pF$

[sorry! Forgot to correct bias to make math work out easier]

b. Estimate the low-frequency input capacitance.

[5] $101 C_\mu + C_\pi = 60pF$

c. Estimate the input capacitance near the unity gain frequency.

[5] $C_\mu + C_\pi = 20.4pF$

d. The same transistor is used in an emitter-follower with a gain of 0.99 . Assuming the same bias conditions, estimate the low-frequency input capacitance.

[5] $C_\mu + 0.01 C_\pi = 0.6pF$

8. You have invented a new type of transistor with 3 terminals, X, Y, and Z. The current into the Y terminal is given by $I_Y = A * \mathrm{sqrt}(V_{XZ} * V_{YZ})$, where A=1mA/V. The current into the X terminal, I_X, is identically 0. The device operates with both V_{XZ} and V_{YZ} between 100mV and 10 V.

a. How would you wire this device up with an ideal current source to make a high gain voltage amplifier? Draw the circuit, and label the nodes on your device.

b. Assuming that the device is biased at an operating point (V^*_{XZ}, V^*_{YZ}, I^*_Y), what is the low-frequency small-signal model for your device? Draw the schematic, and write down an expression for all of the component values.

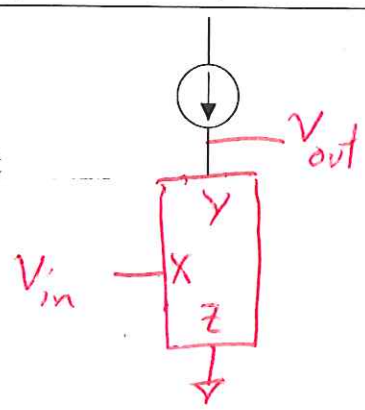
c. Write a formula the small-signal voltage gain for your amplifier in terms of the bias point variables.

d. What bias point would you choose for your amplifier to get maximum gain? Write down the bias voltages and currents, and the resulting gain.

[4]

1 pt per label

Amplifier circuit



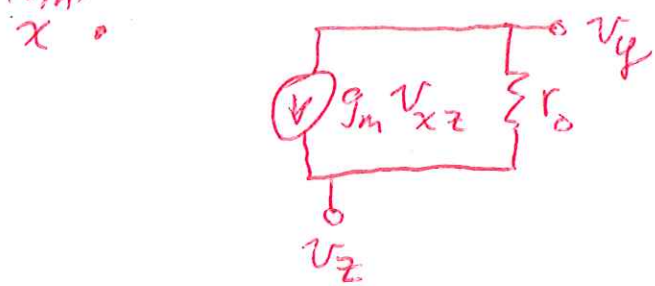
$$g_m = \frac{\partial I_Y}{\partial V_{XZ}} = \frac{1}{2} A \sqrt{\frac{V_{YZ}}{V_{XZ}}}$$

$$g_o = \frac{\partial I_Y}{\partial V_{YZ}} = \frac{1}{2} A \sqrt{\frac{V_{XZ}}{V_{YZ}}}$$

$$r_o = \frac{1}{g_o} = \frac{2}{A} \sqrt{\frac{V_{YZ}}{V_{XZ}}}$$

[4]

Small signal model with formulas



$$g_m = \frac{1}{2} A \sqrt{\frac{V_{YZ}}{V_{XZ}}} = \frac{I_Y}{2 V_{XZ}}$$ [4]

$$r_o = \frac{2}{A} \sqrt{\frac{V_{YZ}}{V_{XZ}}} = \frac{2 V_{YZ}}{I_Y}$$ [4]

[2]

Gain formula

$$A_v = -g_m r_o = \frac{-V_{YZ}}{V_{XZ}}$$

Bias point and gain

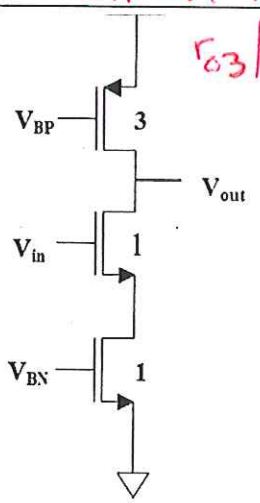
$V^*_{XZ} = 100mV$ [4] $V^*_{YZ} = 10V$ [4] $I_Y = 1mA$ [2] $A_v = -100$ [2]

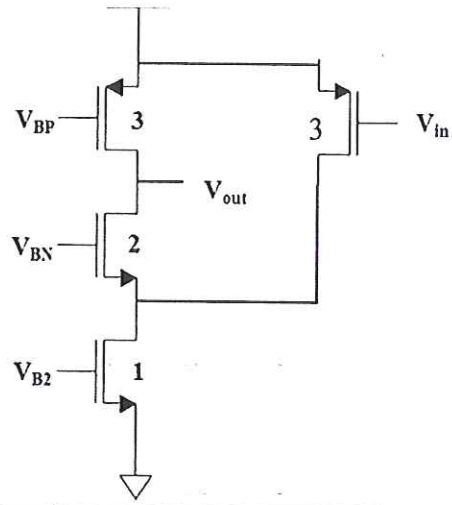
30.

9. Calculate G_M and R_o as indicated for the following circuits. Assume all transistors are in saturation and that $g_m r_o >> 1$ for all combinations. Transistors labeled the same (e.g. 1 and 1) have the same small signal parameters. Write your answers in terms of the specific small signal parameters, e.g. g_{m3}, r_{o2}, etc.

[3] G_m $\frac{g_{m1}}{1+g_{m1}r_{o1}}$ or $\frac{1}{r_{o1}}$

[3] R_o $r_{o3} \| r_{o1}(1+g_{m1}r_{o1})$ or $r_{o3} \| g_{m1}r_{o1}^2$

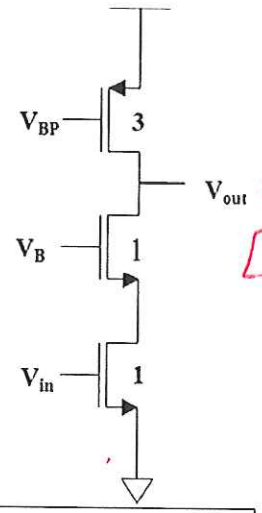




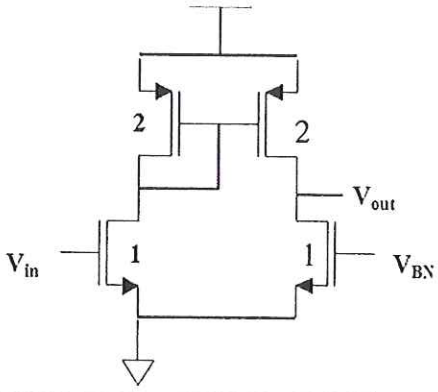
[4] G_m g_{m3}

[4] R_o $r_{o3} \| r_{o2}(1+g_{m2}(r_{o1} \| r_{o3}))$

or $r_{o3} \| g_{m2}r_{o2}(r_{o1} \| r_{o3})$

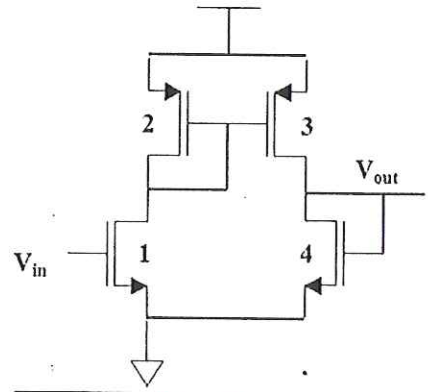


[3] G_m g_{m1}



[3] G_m $-g_{m1}$

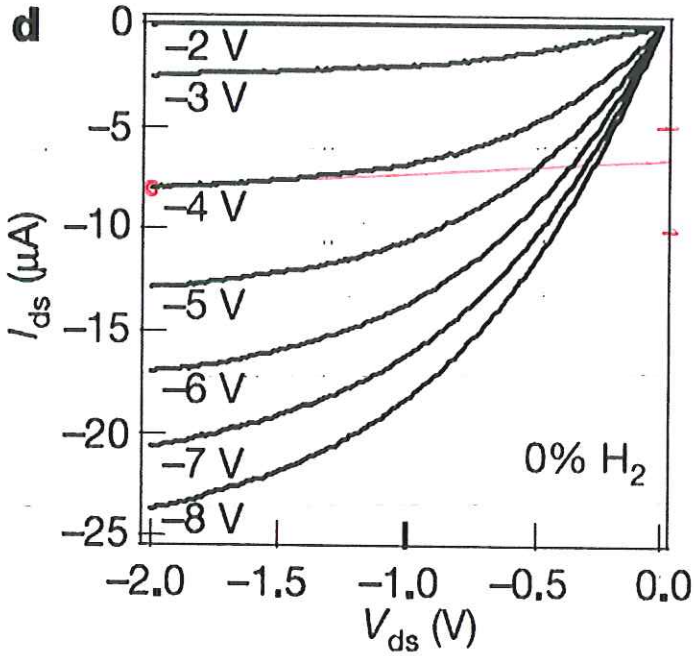
[3] R_o $r_{o2} \| r_{o1}$



[4] G_m $-\frac{g_{m1}g_{m3}}{g_{m2}}$

[3] R_o $\frac{1}{g_{m4}}$ or $r_{o3} \| \frac{1}{g_{m4}}$

10. Before coming to Berkeley, Prof. Ali Javey made the highest performance single-molecule carbon nanotube field-effect transistors on the planet. Here's a graph of their drain current vs. drain-to-source voltage at several different gate-to-source bias points.



$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-5\mu A}{-1V} = 5\mu S$

$g_o = \frac{\Delta I_D}{\Delta V_{DS}} \cong \frac{+1\mu A}{+2V} = \frac{1}{2}\mu S$

$r_o = \frac{1}{g_o} = 2M\Omega$

a. Is this an NMOS or a PMOS FET?

[2] PMOS

b. Estimate the threshold voltage for this device.

[4] −2.5

c. If the device is biased with V_{DS}=-2V, and V_{GS}=-4V, estimate the transconductance, output resistance, and intrinsic gain at this bias point.

g_m	r_o	A_v
5μS	2MΩ	−10 or 10
[5]	[5]	[4]

±5 ~ ±25

g_m Quadratic model calc

e.g. $\frac{2I_D}{V_{DSat}} = \frac{2 \cdot 8\mu A}{2.5V} \cong 7\mu S$ −4

this is not quadratic

r_o

1 − 5 MΩ full credit

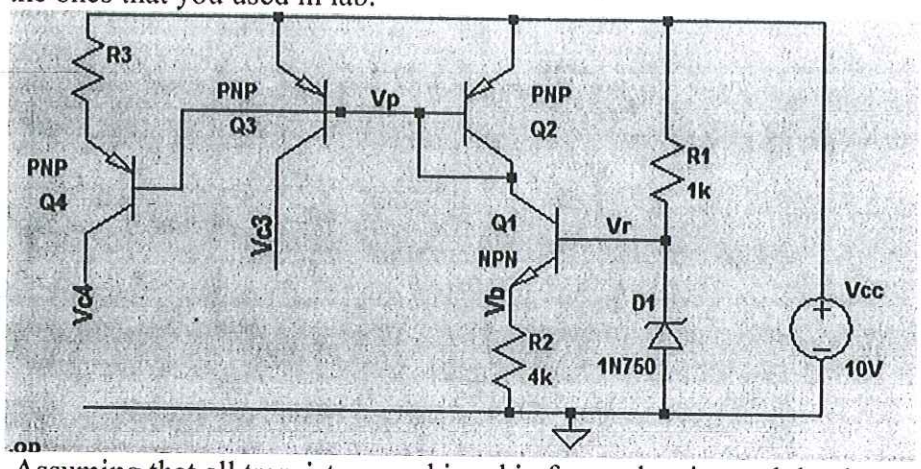
0.5 − 1, 5 − 10 −2

otherwise 0

draw a slope +1

write formula $\left(\frac{\Delta I_D}{\Delta V_{DS}}\right)^{-1}$ +1

11. The circuit below is very similar to the bias circuit from the RC4558 op-amp. The diode D1 is a Zener with a breakdown voltage of 4.7V. The transistors are similar to the ones that you used in lab.



a. Assuming that all transistors are biased in forward active and that beta and V_A are infinite, find the DC bias point of the circuit and fill in the following table.

[20]

Vr	Vb	Vp	I_{R2}	I_{C1}	I_{C2}	I_{C3}	I_{D1}
4.7	4	9.3	1mA	1mA	1mA	1mA	5.3mA
3	3	2	3	2	2	2	3

b. Design R3 to get I_{C4} to be ten times smaller than I_{C3}.

[5]

$I_{R3} = 100\mu A$

$V_{R3} = 60mV$

$R_3 = \frac{60mV}{100\mu A} = 600\Omega$

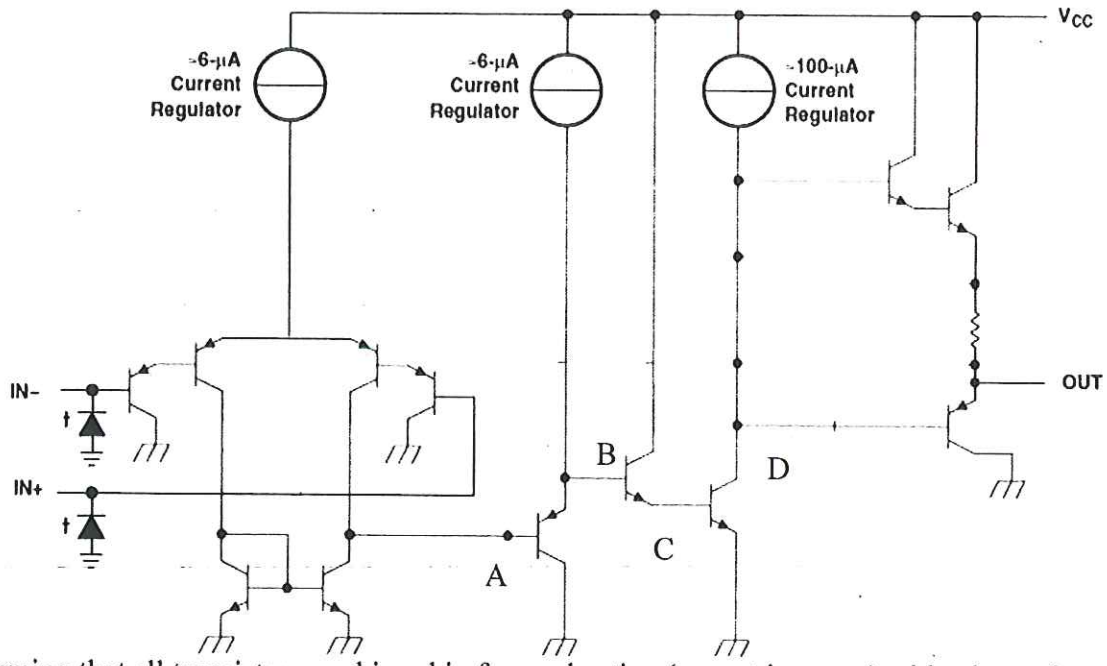
c. If Vcc increases to 20V, would you expect that the magnitude of I_{C3} will: decrease ~2X, decrease less than 10%, stay the same, increase less than 10%, or increase ~2X?

[5]

Stay the same +2

increase 2X +1

12. The circuit below is simplified from the LM324 datasheet. I've changed the device parameters, so your results below won't fit with the numbers in the datasheet.



Assuming that all transistors are biased in forward active (except in part e) with a beta of 100, and V_A=100V, and that the + and – inputs are both biased near mid-rail, and the amplifier is being used in an external circuit that is not shown.

a. Estimate the input current (I_B on one of the input transistors)

$\frac{6\mu A}{2}$ $\frac{1}{\beta^2}$ 0.6nA -1 30nA -2

I_B	0.3nA

[4]

b. Estimate the theoretical maximum source current (positive current into the load)

$100\mu A \cdot \beta^2$ 100µA -3 10mA -2

I_{source}	1A

[4]

c. Estimate the theoretical maximum sink current (negative current pulled out of the load to ground)

600µA -3 60mA -2

$6\mu A \cdot \beta^3$

I_{sink}	6A

[4]

d. Estimate the gain from A to B, B to C, and C to D, assuming that the output current is very small, and the current sources are ideal

BC: 1 -3

AB	1	[4]
BC	1/2	[5]
CD	-4,000	[5]

e. If the op-amp is driving a capacitive load with a 100mV peak-to-peak sine wave centered at Vcc/2, estimate the peak-to-peak amplitude of the waveform at node D. Note that some devices may not remain in forward active.

$3 \times 0.6 + 2 \times 0.1 =$

V_{Dpp}	2V

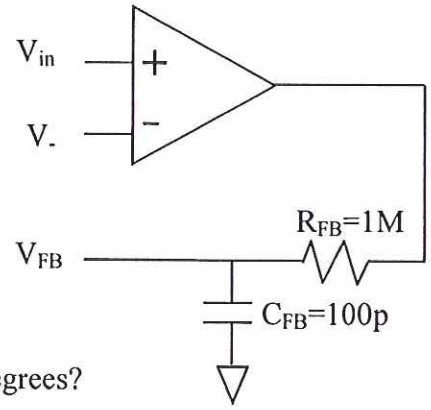
[4]

1.8V -1

2.3V OK

0.2V -3

13. You have built an op-amp with an open-loop gain of 10,000 and two poles at 10^7 rad/sec, and possibly other poles at much higher frequency. You want to put it in unity-gain feedback, but it oscillates, so you need to design a low-pass filter to compensate (stabilize) the closed-loop system. Your amplifier has very high input impedance and very low output impedance.

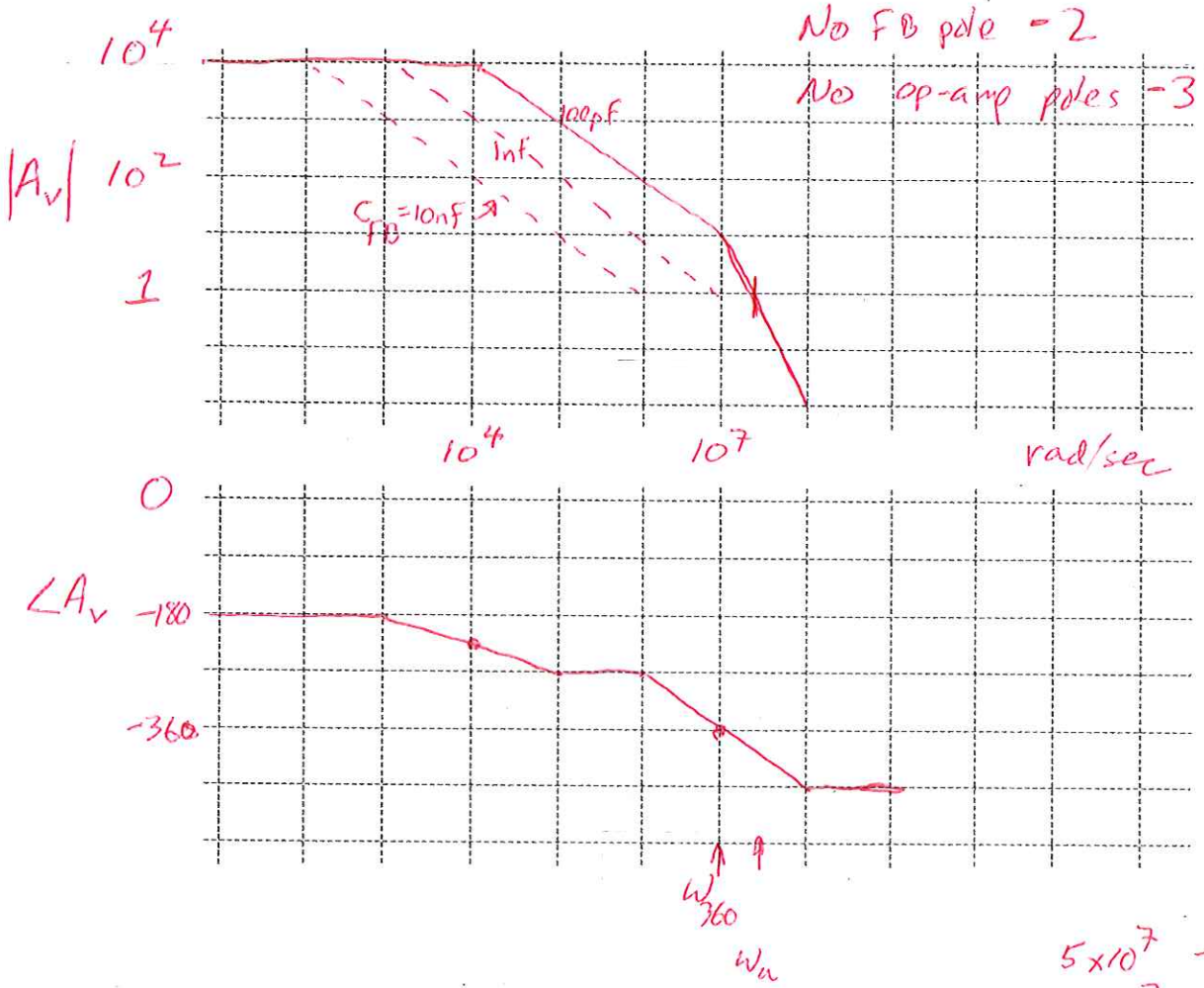


a. What frequency is the feedback pole? [1]

ω_{FB} 10^4

b. Draw a Bode plot of the loop gain from V_- to V_{FB}.
c. What frequency is ω_{360}?
d. What frequency is ω_1?
e. Will the system oscillate in feedback? Why or why not?
f. What is the minimum value of C_{FB} to make the system stable?
g. What value of C_{FB} will give the system a phase margin of 90 degrees?

No FB pole −2
No op-amp poles −3



[5 total]

LABEL ALL AXES!

5×10^7 −2
10^7 −4
10^8 −4

ω_{360} 10^7 rad/sec

ω_1 2×10^7 or 3×10^7

[5 each]

Oscillate? Why? [2] Yes $\omega_{360} < \omega_1$ [3] or $|H(j\omega_{360})| > 1$

Stable C_{FB} 200pF or 300pF −2
1nF

C_{FB} for 90 phase margin 10nF

100 (100pF)
100nF −3
1nF −4