UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105 Prof. Pister
Spring 2011

Homework Assignment #6

Due in the 105 box on the 2nd floor of Cory, 5pm Friday 3/4/2010

Problem 1: For the lab this week you need to write down most or all of Chapter 5 Equations 263, 264, 271, 321, 326, 329. Draw the small signal model of a common base amplifier and derive 5.263 and 5.264

Problem 2: Figure 16.15 shows a CS amplifier with resistive gate bias and capacitive input coupling. You want to be able to amplify audio signals between 20Hz and 20kHz. The microphone has a source impedance of 100kΩ. Assuming $\mu_n C_{ox}=200\mu A/V^2$, $V_{tn}=0.5$, $\lambda=0.1V^{-1}$, and $V_{DD}=1.8V$, design this amplifier to have $I_D=100\mu A$ and a gain of at least 10.
Find the operating point, draw the small signal model, and find the input resistance (as seen by the capacitor), the output resistance, and the gain.
Things to think about:

- The supply voltage and the current set an upper limit on the value of R_D. That and the gain requirement set a lower limit on the value of g_m (why doesn't ro enter into it?). That limit on g_m, combined with the current, sets a limit on the value of V_{DSAT}.
- The source impedance sets a lower limit on the input impedance of the amplifier. That sets a lower limit on the parallel combination of R1 and R2.
- The frequency range and the gate bias resistors will set an upper limit on the impedance of the capacitor. That limit and the frequency range of interest will set a lower limit on the size of the capacitor.

Problem 3: Simulate your amplifier in SPICE: find the operating point and compare to your hand calculations. Make a Bode plot – does it work over the range from 20 to 20k?