Discussion notes: MOS cascode Amplifier.

In this example, we will design the MOS cascode amplifier. The required small-signal specifications are Gm greater or equal to 1mS, Rout greater or equal to 20mΩ.

We want the amplifier to have an output voltage swing vout between 1 and 4V. Assume the current source supply has an infinite internal resistance and requires 1V across it to be in its constant current region.

Use the circuit of Figure Ex9.4 on page 576 of the textbook.

Solution:

We approach this design by trying to achieve the small signal specifications and see if we still meet the large signal voltage swing specification. The transconductance of this cascode is just the transconductance of M1. A wide device is needed to achieve the maximum transconductance. As a starting point, let’s choose (W/L)1=100/2 and set gm1=1mS.

\[ gm_1 = \sqrt{2(W/L)\mu_nCoxI_{sup}} = 1mS \Rightarrow I_{sup} = 200\mu A \]

The output resistance of this cascode can be found by realizing that the cascode is a CS-CG amplifier. By noting that the output resistance of device M1 is acting as the source resistance of the common gate amplifier formed by M2, we can write:

\[ Rout = (ro2 + gm2ro2ro1) = gm2ro2ro1 \]

\[ \lambda_{n1} = \frac{\lambda_n}{2\mu m} = 0.05V^{-1} \]

\[ rol = \frac{1}{\lambda_nI_{sup}} = 100k\Omega \]

If we size M2 the same as M1, we get gm1rol=gm2ro2=100, which gives

\[ Rout = 10M\Omega \]

We need to double the output resistance to achieve the specification for Rout, which can be achieved in a number of ways. However, first we should see how close we are to the voltage swing specification and then decide how to achieve the required Rout.

Given

\[ I_{sup} = 0.2mA \text{ and } (W/L)1=(W/L)2=100/2. \]

\[ V_{bias} = V_{tn} + \sqrt{\frac{2I_{sup}}{(W/L)\mu_nCox}} = 1.4V \]

Note: to ensure that device M1 is operating in the constant current region V_{DS1} must be greater than V_{DSSAT}=V_{bias}-V_{tn}=0.4V. Neglecting backgate effect, we find that M2 will require the same (V_{GS}-V_{tn}), namely 0.4V.
We can find $V_{G2}$ by

$$V_{G2} = V_{tn} + \sqrt{\frac{2I_{sup}}{(W/L)^2\mu_n C_{ox}}} + V_{S2} = 1.8V$$

$$V_{DSsat} = V_{GS2} - V_{Tn} = 0.4V$$

We can swing the output voltage between $V_{DSsat1} + V_{DSsat2}$ and 4V, namely $V_{out}$ can swing between 0.8V and 4V. This meets the voltage swing specification. The channel length of M1 can be double to make the $R_{out}$ specification. This will require that we double the width of M1 to maintain the same $g_m$ and $V_{bias}$. Several other options are also possible such as reducing $I_{sup}$, while increasing $W_1$ and $W_2$.

Our final design has:

(W/L)1=200/4, (W/L)2=100/2, $I_{sup}$=200µA, $V_{bias}$=1.4V and VG2=1.8V.

When the circuit is simulated in SPICE, the results are:

Gm=$g_m$=1.001mS

Rout=24.5MΩ

$V_{DSsat1}$=0.4V

$V_{DSsat2}$=0.38V

Since $V_{DSsat1} + V_{DSsat2}$ is smaller than 1V, we have met our voltage swing specification.