Lecture 9

• Last time:
  – MOS field effect transistor (MOSFET)
  – current-voltage characteristics

• Today:
  – MOSFET sample & hold circuit: linear model
  – Large-signal analysis

Linear MOSFET Model

Channel (inversion) charge: neglect reduction at drain

Velocity saturation defines

\[ V_{DS, SAT} = E_{sat} L = \text{constant} \]

Drain current in saturation:

\[ I_{D, SAT} = -W Q_N = -W (V_{sat}) [ -C_{ox} (V_{GS} - V_{Th}) ] \]

\[ |E_{sat}| = 10^4 \text{ V/cm}, L = 0.12 \mu \text{m} \rightarrow V_{DS, SAT} = 0.12 \text{ V!} \]

“Linear” I-V Characteristics:
short-channel MOSFET

Sample & Hold Function

• Goal: charge up load capacitor to input voltage rapidly when control voltage is switched on; hold voltage on capacitor when control is switched off

• Applications: analog-to-digital converters
Linear Model: $v_s$ small

- Initial condition: $v_I = 0 \text{ V}$
- Gate voltage steps from 0 V to $V_{DD} = 2.5 \text{ V}$

$$i_D = \mu_n C_{ox} (W/L)(v_{GS} - V_T - v_{DS}) v_{DS}$$

Gate-source voltage: $v_{GS} = V_{DD} - v_I$

Drain-source voltage: $v_{DS} = v_s - v_I$

$$i_D \approx \mu_n C_{ox} (W/L)(V_{DD} - V_T)(v_s - v_I)$$

Equivalent Circuit

Example

$\mu C_{ox} = 50 \mu \text{A/V}^2$, $V_{GS} = V_{DD} = 2.5 \text{ V}$, $V_T = 0.5 \text{ V}$, $L = 0.6 \mu\text{m}$

If we want $R_{DS} = 100 \Omega$, then the MOSFET width must be:

$$W = \frac{R_{DS} L}{\mu C_{ox} (V_{DD} - V_T)} = \frac{0.6}{100 \times 50 \times 10^{-9} \times 2} = 60 \mu\text{m}$$

For an efficient layout, this transistor with $W/L = 100$ should be folded ... see example in Chapter 4.

Example Waveform

$$v_I(t) = v_I (1 - e^{-t/R_{DS} C_s})$$

$0.6(50) = 31.5\text{ mV}$
Sampling Error

Absolute error = \( e = v_i - v_s \)

Relative error = \( \varepsilon = e / v_s \)

\[
\varepsilon = \frac{v_i - v_s}{v_s} \left(1 - e^{-t_i / R_D \mu} \right)
\]

where \( t_i \) is the sampling time (time interval where \( V_{GS} = V_{DD} \))

\[
\varepsilon = e^{-t_i / R_D \mu}
\]

Example case: \( R_D = 100 \Omega, C_L = 500 \text{ fF} \rightarrow \tau = 50 \text{ ps} \)

For 16 bit precision, we need the relative error \( \varepsilon \) \(< 2^{-16} = 1.5 \times 10^{-5} = 15 \text{ ppm (parts per million)} \)

\( t_s = -\tau \ln(\varepsilon) = \tau(1.1) = 554 \text{ ps} \)

Sampling Large Voltages

If the source (a.k.a. input) voltage is not small \( \rightarrow \) need to use the full model for the MOSFET

\[
v_{DS} = V_{DD} - V_L > V_{ID} - V_L - V_T = V_{GS} \rightarrow \text{saturated,}
\]

as long as \( V_{GS} > V_T \)

\[
\begin{align*}
\dot{i}_d(t) &= \frac{K_{C_m}}{2}(W/L)(v_{GS} - V_T)^2 = K(v_{DD} - V_T - V_T)^2 \\
\int_0^t \dot{i}_d(t) dt' &= \int_0^t \frac{C_L}{K(v_{DD} - V_T - V_T)^2} dt' = \frac{C_L}{K(v_{DD} - V_T - V_T)^2} \int_0^t \frac{C_L}{K(v_{DD} - V_T - V_T)^2} dt' \\
\end{align*}
\]

Solve for Load Voltage

\[
\begin{align*}
\int_0^t \dot{i}_d(t) dt' &= t = \int_0^{v_L} \frac{C_L}{K(v_{DD} - V_T - V_T)^2} dt' = \frac{C_L}{K(v_{DD} - V_T - V_T)^2} \int_0^{v_L} \frac{C_L}{K(v_{DD} - V_T - V_T)^2} dt' \\
\end{align*}
\]

\[
v_L(t) = \frac{K(v_{DD} - V_D)^2 t}{K(v_{DD} - V_T)^2 + C_L} = \left[ \frac{K(v_{DD} - V_D)^2 t}{K(v_{DD} - V_T)^2 + C_L} \right] \left[ 1 + \left( C_L \dot{i}_d(t) \right) \right]
\]

Sampled Voltage Waveform

\[
\begin{align*}
\dot{i}_d(t) &= \frac{K_{C_m}}{2}(W/L)(v_{GS} - V_T)^2 \\
\int_0^t \dot{i}_d(t) dt' &= \int_0^t \frac{C_L}{K(v_{DD} - V_T - V_T)^2} dt' = \frac{C_L}{K(v_{DD} - V_T - V_T)^2} \int_0^t \frac{C_L}{K(v_{DD} - V_T - V_T)^2} dt' \\
\end{align*}
\]

\( v_L \) approaches \( V_{DD} - V_T = 1.5 \text{ V (for } v_s = V_{DD}) \)

\( \mu C_m = 50 \mu \text{A}/\sqrt{\text{V}}, (W/L) = 100 \rightarrow \dot{i}_d(t = 0) = 5.6 \text{ mA} \)
Improved Sample and Hold

NMOS and PMOS transistors in parallel → sampled voltage can be pulled up to the supply voltage and pulled down to ground.