Lecture 29

• Last time:
  – Transistor action, large-signal operation

• Today:
  – Ebers-Moll model
  – Small-signal model of the npn bipolar transistor

Transconductance (cont.)

• Forward-active large-signal current:
  \[ i_C = I_S e^{\frac{V_{BE}}{V_{th}}} \left( 1 + \frac{V_{CE}}{V_A} \right) \]

• Differentiating and evaluating at \( Q = (V_{BE}, V_{CE}) \)

Comparison with MOSFET \( g_m \)

• Bipolar transistor:
  • Typical bias point: drain/coll. current = 100 \( \mu \text{A} \);
    Select \( W/L = 8/1, \mu_n C_{ox} = 100 \mu \text{A/V}^2 \)

• MOSFET:

What about the Base Current?

Unlike MOSFET, there is a DC current into the base terminal of a bipolar transistor:

\[ I_B = I_C / \beta_F = (I_S / \beta_F) e^{\frac{V_{BE}}{V_{th}}} \left( 1 + \frac{V_{CE}}{V_{th}} \right) \]

To find the change in base current due to change in base-emitter voltage:

\[ \frac{\partial i_B}{\partial V_{BE}} \bigg|_Q = \frac{\partial i_B}{\partial i_C} \bigg|_Q \frac{\partial i_C}{\partial V_{BE}} \bigg|_Q = \]
Small-Signal Current Gain $\beta_o$

In practice, the DC current gain $\beta_F$ and the small-signal current gain $\beta_o$ are both highly variable (+/- 25%)

Typical bias point: DC collector current = 100 $\mu$A

Output Resistance $r_o$

Why does current increase slightly with increasing $v_{CE}$?

Model: math is a mess, so introduce the Early voltage

$$i_C = I_S e^{v_{BE}/V_A} (1 + v_{CE}/V_A)$$

Input Resistance $r_\pi$

$$(r_\pi)^{-1} = \frac{\partial i_B}{\partial v_{BE}}$$

In practice, the DC current gain $\beta_F$ and the small-signal current gain $\beta_o$ are both highly variable (+/- 25%)

Typical bias point: DC collector current = 100 $\mu$A

Graphical Interpretation of $r_o$

Typical value:
BJT Capacitances

Base-charging capacitance $C_b$: due to minority carrier charge storage (mostly electrons in the base)

$$ C_b = g_m \tau_F $$

Base-emitter depletion capacitance: $C_{JE} = 1.4 \ C_{JE0}$

Total B-E capacitance: $C_{\pi} = C_{JE} + C_b$
SiGe BJT/CMOS vs. RF CMOS

IBM SiGe vs. RF CMOS
SiGe is well-suited for applications that require high speed, low power consumption, high RF linearity, and fast time-to-market. RF CMOS is ideal for lower-performance RF applications that have lower cost requirements.

From “IBM and Cadence collaborate to accelerate silicon-accurate design of advanced RF integrated circuits,” IBM Microelectronics Division, March 11, 2005.

Figure 2

Cutoff frequency $f_T$ vs. $I_C$ for four lithographic generations of SiGe. The InP curve shows recent production InP results.