Lecture 24

• Last time:
  – Multi-stage amplifiers: voltage, transconductance

• Today:
  – Cascode: merged CS/CG cascade
CG Cascade: Sharing a Supply

First stage has no current supply of its own $\Rightarrow$ its output resistance is modified
Multistage Amplifier Design Examples

Start with basic two-stage transconductance amplifier:

CS (NMOS)  

CS (PMOS)

Why do this combination?
Two-Stage Amplifier Topology

Direct DC connection: use NMOS then PMOS

\[ V^+ = +2.5 \text{ V} \]

\[ V^- = -2.5 \text{ V} \]
Current Supply Design

Assume that the reference is a “sink” set by a resistor

Must mirror the reference current and generate a sink for $i_{SUP2}$
Use Basic Current Supplies

\[ V^+ = +2.5\, \text{V} \]

\[ V^- = -2.5\, \text{V} \]
Complete Amplifier Topology

What’s missing? The device dimensions and the bias voltage and reference resistor.
The Cascode Configuration

Common source / common gate cascade is one version of a *cascode* (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own
Cascode Two-Port Model

Output resistance of first stage = $R_{out,CS^*} = R_{down,CS} = r_{o1}$

Why is the cascode such an important configuration?
Miller Capacitance of Input Stage

Find the Miller capacitance for $C_{gd1}$

Input resistance to common-gate second stage is low $\rightarrow$ gain across $C_{gd1}$ is small.
Two-Port Model with Capacitors

Miller capacitance: \( C_M = (1 - A_v C_{gd1}) C_{gd1} \)
Other Cascode Configurations

Basic configuration: transconductance stage followed by current buffer

$CE_n-CG_n$   $CS_n-CB$   $CS_p-CG_p$