Lecture 23

- Last time:
  - Frequency response of voltage and current buffers

- Today:
  - Start multi-stage amplifiers

Multistage Amplifiers

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD

What are the constraints?

1. Input/output resistance matching
2. DC coupling (no passive elements to block the signal)
   … why not?

Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination “works”

Results: \( R_{in} = R_{in1}, \ R_{out} = R_{out2}, A_v = \)

Using CMOS Stages

Input resistance:
Voltage gain (2-port parameter):
Output resistance:
Multistage Current Buffers

Are two cascaded common-base stages better than one?

Input resistance: $R_{in} = R_{in1}$

Summary of Cascaded Amplifiers

General goals:
1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

Voltage: $R_{in}$, $R_{out}$
Current: $R_{in}$, $R_{out}$
Transconductance:
Transresistance:

Common-Gate 2nd Stage

$R_{out} = R_{out2} \cong r_{o2} (1 + g_{m2} R_{S2}) || r_{oc2}$

Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available
Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?
Alternative CG-CC Cascade

Use a PMOS CD Stage: DC level shifts upward

CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case: $I_{BLAS} = 0$ A

CG Cascade: Sharing a Supply

First stage has no current supply of its own $\rightarrow$ its output resistance is modified