1.0 Objective

This experiment will introduce techniques for current source biasing. Several different current sources will be considered. Some requirements for current sources include high output resistance with a wide range of voltage drops and independence from external factors such as supply variation or temperature variation. The second kind of source we’ll be considering is a voltage source. MOS current sources often are biased from a voltage source. An independent voltage source is important to keep a current source properly biased without any variations.

To show your understanding of the lab, your write-up should contain:

- A discussion on the different types of current sources
- A discussion on the choosing the right type of current source
- A discussion on the valid range of operation for various current sources

2.0 Prelab

- H & S: Chapter 9.4
- For the current sources in Figs. 1 and 2, what is $I_{\text{REF}}$, $I_{\text{OUT}}$, the current supply’s internal resistance (in terms of small signal parameters) and the minimum output voltage required to have the circuit act as a current source. Let $R_{\text{REF}}=1 \, \text{k}\Omega$.
- For the circuit in Fig. 4, determine the current through $R_{\text{REF}}$ if all the devices have $W/L=1$. Use your measured values for $K_n$ and $K_p$. Let $R_{\text{REF}}=1 \, \text{k}\Omega$ and ignore the back-gate effect.
3.0 Procedure

3.1 Simple Current Source

1. Construct the circuit in Fig. 1. Let \( R_{REF} = 5 \, \text{k}\Omega \). Find and record the current \( I_{REF} \).

![Simple Current Source (SBSOURCE, Lab Chip 4)](image)

2. Vary the output voltage from 0 to 5 V and measure the current \( I_{SUP} \) from the voltage drop across the 1 k\( \Omega \) resistor. You should record several points below 0.5 V in order to observe saturation effects. Use a 100 \( \Omega \) resistor if the supply voltage is unsteady.

3. Plot \( I_{SUP} \) vs. \( V_{OUT} \) and \( I_{SUP} \) vs. \( V_{CC} - V_{OUT} = V_{SUP} \). Compare the results with SPICE.

4. From the plot, find the output resistance.

3.2 Cascode Current Source

1. Load the default FET \( I_d - V_{ds} \) program.

2. On the first page, change the definition of SUM4 (\( V_{sub} \)) to constant voltage (instead of common). Delete the definition for SMU3.

3. Press Next Page twice to go to the Measurement page. Here, set SMU2 (\( V_d \)) to sweep from 0 to 5V. Set SMU4 (\( V_{sub} \)) to be 5V.

4. Connect SMU1 to pin 14, SMU2 to pin 25, and SMU4 to pin 28. Also, connect the \( R_{ref} \) (1 k\( \Omega \)) between pin 28 and 24. The sweeping voltage on SMU2 provides \( V_{output} \), so you don’t need an external voltage source.
5. Press *Single* to take a measurement. You are plotting $I_d$ vs $V_{ds}$, both at SMU2, which in this case are $I_{sup}$ and $V_{output}$.

6. Execute the program to obtain the plot of the cascode’s $I-V$ characteristics.

7. Using the Marker and Cursor, find the output resistance. (refer to Exp. 1 if you have forgotten how to find the slope of a line.)

8. Note the minimum operating voltage for this current source.

9. How does the cascode compare with the simple current source?

10. Obtain a hardcopy of your data.
3.3 **Totem Pole Voltage Source**

The following schematic shows a totem pole voltage source.
Procedure

1. Construct the circuit by placing a 1 kΩ resistor for $R_{REF}$ between $V_{REF1}$ and $V_{REF2}$. Measure the drain current and the reference voltages.

2. How do the reference voltages compare with theoretical values? How can you account for the difference?

3. The reference voltages act like batteries. Their values remain constant as long as there are no leakage currents at that node. For the NMOS transistor shown in figure 5, use $V_{REF2}$ to generate a reference current, $I_{OUT}$. Vary $V_{OUT}$ and determine the minimum output voltage of this NMOS current source. What is the output resistance?

4. Replace the NMOS with one with a different $W/L$ ratio on Lab Chip 1 (Drain = PIN 6, Gate = PIN 7, Source = PIN 8, and $W/L=46.5/3$) and repeat procedure 3. How do the results compare?

FIGURE 5. NMOS Transistor as a Current Source (Lab Chip 1)
4.0 Optional Experiments

4.1 Resistor Ratioed Current Source

1. Construct the current mirror shown below (devices on Lab Chip 2).

   ![Resistor Ratioed Current Source Diagram]

   FIGURE 6.
   Resistor Ratioed Current Source

1. Let $R_1 = R_2 = 100\,\Omega$ and $R_{REF} = 5\,k\Omega$.

2. Record values for $I_{SUP}$, $V_{BE1}$, and $V_{BE2}$.

3. Change the value of resistor $R_2$ to $1\,k\Omega$. What is $I_{OUT}$?

4. Now switch the resistors. What is $I_{SUP}$ now?

5. Derive an approximate relationship between $I_{SUP}$ and $I_{REF}$. Does your data follow this relationship?

6. Let $R_1 = 1k\Omega$ and $R_2$ be $100\,\Omega$, $3k\Omega$, followed by $5k\Omega$. This should give you better insight into how this mirror works. You need not take a detailed sweep here.

4.2 Totem Pole Voltage Source

1. The reference voltages act like batteries. Their values remain constant as long as there are no leakage currents at that node. For the NMOS transistor shown in figure 5, use $V_{REF}$ to generate a reference current, $I_{SUP}$. Vary $V_{OUT}$ and determine the minimum output voltage of this NMOS current source. What is the output resistance?
2. Replace the NMOS with one with a different $W/L$ ratio on Lab Chip 1 (Drain = PIN 6, Gate = PIN 7, Source = PIN 8, and $W/L=46.5/3$) and repeat procedure 3. How do the results compare?