Final Exam

- Covers the course from the beginning
- Date/Time: SATURDAY, MAY 15, 2004 8-11A
- Location: BECHTEL auditorium
- One page (Two sides) of notes

Observed Behavior: \( I_D - V_{DS} \)

- For low values of drain voltage, the device is like a resistor
- As the voltage is increases, the resistance behaves non-linearly and the rate of increase of current slows
- Eventually the current stops growing and remains essentially constant (current source)

- As the drain voltage increases, the E field across the oxide at the drain end is reduced, and so the charge is less, and the current no longer increases proportionally. As the gate-source voltage is increased, this happens at higher and higher drain voltages.
- The start of the saturation region is shaped like a parabola
Finding $I_D = f(V_{GS}, V_{DS})$

- Approximate inversion charge $Q_N(y)$: drain is higher than the source $\Rightarrow$ less charge at drain end of channel

\[
Q_N(y) \approx Q_N(y = 0) + Q_N(y = L) \approx \frac{1}{2} \left( -C_{ox} (V_{GS} - V_{Th}) - C_{ox} (V_{GD} - V_{Th}) \right)
\]

\[
V_{GD} = V_{GS} - V_{DS}
\]

Average Inversion Charge

- Source End

\[
Q_N(y) = -\frac{C_{ox}(V_{GS} - V_{Th}) + C_{ox}(V_{GD} - V_{Th})}{2}
\]

- Drain End

\[
Q_N(y) = -\frac{C_{ox}(V_{GD} - V_{Th}) + C_{ox}(V_{DS} - V_{Th})}{2}
\]

\[
Q_N(y) = -\frac{C_{ox}(2V_{GS} - 2V_{Th}) - C_{ox}V_{GS} - C_{ox}V_{DS}}{2}
\]

- Charge at drain end is lower since field is lower
- Notice that this only works if the gate is inverted along its entire length
- If there is an inversion along the entire gate, it works well because $Q$ is proportional to $V$ everywhere the gate is inverted

Drift Velocity and Drain Current

“Long-channel” assumption: use mobility to find $v$

\[
v(y) = -\mu(y)(-\Delta V / \Delta y) = -\mu_y \frac{V_{ox}}{L}
\]

And now the current is just charge per area, times velocity, times the width:

\[
I_D = \frac{W}{L} \mu(y)(V_{GS} - V_{Th} - \frac{V_{ox}}{2})
\]

\[
I_D = \frac{W}{L} \mu(y)(V_{GD} - V_{Th} - \frac{V_{ox}}{2})
\]

Inverted Parabolas
Square-Law Characteristics

Boundary: what is $I_{DS,ST}$?

TRIODE REGION

SATURATION REGION

The Saturation Region

When $V_{DS} > V_{GS} - V_{Th}$, there isn’t any inversion charge at the drain ... according to our simplistic model

Why do curves flatten out?

Square-Law Current in Saturation

Current stays at maximum (where $V_{DS} = V_{GS} - V_{Th}$)

$$I_D = \frac{W}{L} \mu C_{ox} (V_{GS} - V_{T}) \frac{V_{DS}}{2}$$

$$I_{DS,sat} = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{T} - \frac{V_{DS}}{2} \right)$$

Measurement: $I_D$ increases slightly with increasing $V_{DS}$ model with linear “fudge factor”

$$I_{DS,sat} = \frac{W}{L} \mu C_{ox} (V_{GS} - V_{T}) \left( 1 + \alpha V_{DS} \right)$$

A Simple Circuit: An MOS Amplifier

Input signal  
Supply “Rail”

Output signal

$$V_{GS} = V_{GS} + V_i$$

$$V_{DS} = V_{DS}$$

$$V_o$$

$$R_o$$

$V_{DS}$

$V_i$
Small Signal Analysis

- Step 1: Find DC operating point. Calculate (estimate) the DC voltages and currents (ignore small signals sources)
- Substitute the small-signal model of the MOSFET/BJT/Diode and the small-signal models of the other circuit elements.
- Solve for desired parameters (gain, input impedance, …)

A Simple Circuit: An MOS Amplifier

\[ v_{GS} = V_{GS} + v_i \]

Input signal

Output signal

Small-Signal Modeling

Step 1. Find DC Bias – ignore small-signal source

What are the small-signal models of the DC supplies?

Shorts!
Small-Signal Models of Ideal Supplies

Small-signal model:

\[ g_{\text{supply}} = \frac{\partial i_{\text{supply}}}{\partial v_{\text{supply}}} = \infty \]

\[ r_{\text{supply}} = \infty \]

short

open

Low-Frequency Voltage Gain

Consider first \( \omega \to 0 \) case … capacitors are open-circuits

\[ v_{\text{out}} = -g_m v_m \left( R_D \parallel r_o \right) \]

\[ A_v = -g_m \left( R_D \parallel r_o \right) \]

Transconductance

\[ g_m = \mu_C \frac{W}{L} \frac{V_{GS} - V_T}{V_{GS} - V_T} \]

Design Variables

Voltage Gain (Cont.)

Substitute transconductance:

\[ A_v = \left( -\frac{2I_{D,SAT}}{V_{GS} - V_T} \right) \left( R_D \parallel r_o \right) g_m R_D \]

Output resistance: typical value \( \lambda_n = 0.05 \text{ V}^{-1} \)

\[ r_p = \left( \frac{1}{\lambda_n I_{D,SAT}} \right) = \left( \frac{1}{0.05 \cdot 0.1} \right) \text{k}\Omega = 200 \text{k}\Omega \]

Voltage gain:

\[ A_v = \left( -\frac{2 \cdot 0.1}{0.32} \right) \left( 25 \parallel 200 \right) = -14.3 \]
**Input and Output Waveforms**

- Output small-signal voltage amplitude: \(14 \times 25 \text{ mV} = 350\)
- Input small-signal voltage amplitude: \(25 \text{ mV}\)

**Maximum Output Amplitude**

\[v_{\text{out}}(t) = -2.18 \cos(\omega t) \Rightarrow v_x(t) = 152 \text{ mV} \cos(\omega t)\]

How accurate is the small-signal (linear) model?

\[
\frac{v_x}{V_{GS} - V_{TH}} = \frac{0.152}{0.32} \approx 0.5
\]

Significant error in neglecting third term in expansion of \(i_D = i_D(v_{GS})\)

**What Limits the Output Amplitude?**

1. \(v_{\text{OUT}}(t)\) reaches \(V_{\text{SUP}}\) or \(0\) … or

2. MOSFET leaves constant-current region and enters triode region

\[V_{DS} \leq V_{DS,SAT} = V_{GS} - V_{TH} = 0.31 \text{ V}\]

\[v_o,\text{MIN} = V_{DS,SAT} = 0.32 \text{ V}\]

\[\text{amp} = 2.5 - 0.32 \text{V} = 2.18 \text{V}\]

**One-Port Models (EECS 40)**

- A terminal pair across which a voltage and associated current are defined

\[
\begin{align*}
\text{Circuit} & + & i_{ab} \\
\text{Block} & - & v_{ab}
\end{align*}
\]
Small-Signal Two-Port Models

- We assume that input port is linear and that the amplifier is unilateral:
  - Output depends on input but input is independent of output.
- Output port: depends linearly on the current and voltage at the input and output ports
- Unilateral assumption is good as long as “overlap” capacitance is small (MOS)

Two-Port Small-Signal Amplifiers

- Voltage Amplifier
- Current Amplifier

Common-Source Amplifier (again)

How to isolate DC level?
**DC Bias**

Neglect all AC signals

\[ V_{DD} = 5 \text{ V} \]

\[ V_{OUT} = 2.5 \text{ V} \]

Choose \( I_{BIB}, \frac{W}{L} \)

**Small-Signal Analysis**

**Load-Line Analysis to find \( Q \)**

\[ I_D = \frac{V_{BIB} - V_{OUT}}{R_D} \]

\[ V_{BIB} (V) \text{ vs. } I_D (\text{mA}) \]

\[ \text{slope} = \frac{1}{10k} \]

**Two-Port Parameters:**

Find \( R_{in}, R_{out}, G_m \)

\[ G_m = \frac{g_m}{R_s} \]

\[ R_{out} = \frac{V_{OUT}}{I_D} \]
Two-Port CS Model

Reattach source and load one-ports:

Maximize Gain of CS Amp

\[ A_v = -g_m R_D \parallel r_o \]

- Increase the \( g_m \) (more current)
- Increase \( R_D \) (free? Don’t need to dissipate extra power)
- Limit: Must keep the device in saturation

\[ V_{DS} = V_{DD} - I_D R_D > V_{DS,\text{sat}} \]

- For a fixed current, the load resistor can only be chosen so large
- To have good swing we’d also like to avoid getting too close to saturation

Current Source Supply

- Solution: Use a current source!
- Current independent of voltage for ideal source

CS Amp with Current Source Supply
Load Line for DC Biasing

Both the I-source and the transistor are idealized for DC bias analysis.

Two-Port Parameters

From current source supply

\[ R_{in} = \infty \]
\[ G_{in} = g_{m} \]
\[ R_{out} = r_{o} \parallel r_{dc} \]

P-Channel CS Amplifier

DC bias: \( V_{SG} = V_{DD} - V_{BIAS} \) sets drain current \(-I_{DP} = I_{SUP}\)
Common Gate Amplifier

DC bias:

\[ I_{SUP} = I_{BIAS} = I_{DS} \]

Gain of transistor tends to hold this node at ss ground: low input impedance load for current input

Notice that \( I_{DS} \) must equal \( -I_i \)

CG as a Current Amplifier: Find \( A_i \)

\[ i_{out} = i_d = -i_i \]

\[ A_i = -1 \]

CG Input Resistance

At input:

\[ i_i = -g_{m}r_{m}v_{gs} + g_{m}v_{gs} + \left( \frac{v_{gs} - v_{gs}}{r_{m}} \right) \]

Output voltage:

\[ v_{out} = -i_i (r_{o} || R_i) = i_i (r_{o} || R_i) \]

\[ i_i = g_{m}v_{gs} + g_{m}v_{gs} + \left( \frac{v_{gs} - v_{gs}}{r_{m}} \right) \]

Approximations...

- We have this messy result

\[ \frac{1}{R_m} = \frac{i_i}{v_i} = \frac{g_m + R_{m} + \frac{1}{r_o}}{1 + \frac{r_o}{r_i} || R_i} \]

- But we don’t need that much precision. Let’s start approximating:

\[ g_{m} + R_{m} >> \frac{1}{r_o} \quad r_{m} || R_i \approx R_i \quad \frac{R_i}{r_o} \approx 0 \]

\[ R_m = \frac{1}{g_m + g_{m} || R_{m}} \]
CG Output Resistance

\[ \frac{V_v}{R_s} - g_m V_o - (-g_m V_v) + \frac{V_v - V_o}{r_o} = 0 \]

\[ V_v \left( \frac{1}{R_s} + g_m + g_m + \frac{1}{r_o} \right) = \frac{V_v}{r_o} \]

Substituting \( V_s = i_s R_S \)

\[ i_s R_s \left( \frac{1}{R_s} + g_m + g_m + \frac{1}{r_o} \right) = \frac{V_v}{r_o} \]

The output resistance is \( (v_i / i_i) \parallel r_{oc} \)

\[ R_{out} = r_{oc} \parallel \left( R_s \left( \frac{R_m + g_m r_o + g_m r_o + 1}{R_s} \right) \right) \]

Approximating the CG \( R_{out} \)

\[ R_{out} = r_{oc} \parallel [r_o + g_m r_o R_S + g_m r_o R_S + R_S] \]

The exact result is complicated, so let’s try to make it simpler:

\[ g_m \approx 500 \mu S \quad g_m \approx 50 \mu S \quad r_o \approx 200 k\Omega \]

\[ R_{out} \approx r_{oc} \parallel [r_o + g_m r_o R_S + R_S] \]

Assuming the source resistance is less than \( r_{oc} \),

\[ R_{out} \approx r_{oc} \parallel [r_o + g_m r_o R_S] = r_{oc} \parallel [r_o (1 + g_m R_S)] \]

CG Two-Port Model

Function: a current buffer

- Low Input Impedance
- High Output Impedance
Common-Drain Amplifier

In the common drain amp, the output is taken from a terminal of which the current is a sensitive function.

\[ I_{DS} = \mu C_{ox} W \frac{1}{2} \left( V_{GS} - V_T \right)^2 \]

*Weak \( I_{DS} \) dependence*

CD Voltage Gain

KCL at source node:

\[ \frac{V_{DS}}{r_o} = g_m \left( V_i - V_{out} \right) - g_{os} V_{out} \]

\[ \frac{1}{r_o || r_e} + g_{os} + g_m \]

Voltage gain (for \( V_{SB} \) not zero):

\[ \frac{V_{in}}{V_{in}} = \frac{g_m}{r_e || r_o} + g_{os} + g_m \approx 1 \]

CD Output Resistance

Sum currents at output (source) node:

\[ R_{out} = r_e || r_o \frac{V_i}{i_i} = g_m V_i + g_{os} V_i \]

\[ R_{out} \approx \frac{1}{g_m + g_{os}} \]
CD Output Resistance (Cont.)

\[ r_o \parallel r_{oC} \text{ is much larger than the inverses of the transconductances } \rightarrow \text{ ignore} \]

\[ R_{\text{out}} = \frac{1}{g_m + g_{oc}} \]

Function: a voltage buffer
- High Input Impedance
- Low Output Impedance

Bias sensitivity
- When a transistor biasing circuit is designed, it is important to realize that the characteristics of the transistor can vary widely, and that passive components vary significantly also.
- Biasing circuits must therefore be designed to produce a usable bias without counting on specific values for these components.
- One example is a BJT base bias in a CE amp. A slight change in the base-emitter voltage makes a very large difference in the quiescent point. The insertion of a resistor at the emitter will improve sensitivity.

Insensitivity to transistor parameters
- Most of the circuit parameters are independent of variation of the transistor parameters, and depend only on resistance ratios. That is often a design goal, but in integrated circuits we will not want to use so many resistors.
NMOS pullup

• Rather than using a big (and expensive) resistor, let’s look at a NMOS transistor as an active pullup device.

\[ I_D = \left( \frac{W}{2L} \right) \mu C_m (V_{SD} - V_{th}) (1 + \lambda V_{SD}) \]

Note that when the transistor is connected this way, it is not an amplifier, it is a two terminal device. When the gate is connected to the drain of this NMOS device, it will be in saturation, so we get the equation for the drain current:

IV for NMOS pull-up

• The I-V characteristic of this pull-up device:

\[ I_D = \left( \frac{W}{2L} \right) \mu C_m (V_{SD} - V_{th}) (1 + \lambda V_{SD}) \]

Active Load

• We can use this as the pullup device for an NMOS common source amplifier:

\[ I_{D1} = \left( \frac{W}{2L} \right) \mu C_m (V_{g1} - V_{th}) \]
\[ I_{D2} = \left( \frac{W}{2L} \right) \mu C_m (V_{g2} - V_{th}) \]

\[ V_O = V_{DD} - V_{g2} \]
\[ V_S = V_{DD} - V_{g1} - \frac{2L}{\mu C_m (W_1 / L_1)} \]

Small signal model

• So we have:

\[ I_D = \left( \frac{W}{2L} \right) \mu C_m (V_{SD} - V_{th}) (1 + \lambda V_{SD}) \]
\[ I_D = \left( \frac{W}{2L} \right) \mu C_m (V_{SD} - V_{th}) (1 + \lambda V_{SD}) \]

• The N channel MOSFET’s transconductance is:

\[ g_m = \frac{\partial I_D}{\partial V_D} \rightarrow \mu C_m (V_{SD} - V_{th}) \approx \left( \frac{W}{2L} \right) \mu C_m (V_{SD} - V_{th}) \]

• And so the small signal model for this device will be a resistor with a resistance:

\[ R = \frac{1}{g_m} \]
Active Load

Since $I_2 = I_1$ we have:

$$V_D = V_{DD} - V_{D2} - \frac{2I_1}{\mu_C W_2 L_2}$$

And since: $V_{gs1} = V_i$

$$V_D = V_{DD} - V_{in} - \frac{W_1}{W_2} L_1 (V_i - V_n)$$

CMOS Diode Connected Transistor

- Short gate/drain of a transistor and pass current through it
- Since $V GS = V DS$, the device is in saturation since $V DS > V GS - V T$
- Since FET is a square-law (or weaker) device, the I-V curve is very soft compared to PN junction diode

Behavior

- If the output voltage goes higher than one threshold below $V DD$, transistor 2 goes into cutoff and the amplifier will clip.
- If the output goes too low, then transistor 1 will fall out of the saturation mode.
- Within these limitations, this stage gives a good linear amplification.

Diode Equivalent Circuit

$$R_D = \left( \frac{dI_{OUT}}{dV_{OUT}} \right)_{i_{OUT}=0}^{-1} = \frac{V_D}{I_i}$$

$$R_D \approx \frac{1}{g_m}$$

Equivalent Circuit:
The Integrated “Current Mirror”

- M₁ and M₂ have the same \( V_{GS} \).
- If we neglect CLM (\( \lambda = 0 \)), then the drain currents are equal.
- Since \( \lambda \) is small, the currents will nearly mirror one another even if \( V_{out} \) is not equal to \( V_{GS1} \).
- We say that the current \( I_{REF} \) is mirrored into \( i_{OUT} \).
- Notice that the mirror works for small and large signals!

Current Mirror as Current Sink

- The output current of M₂ is only weakly dependent on \( V_{OUT} \) due to high output resistance of FET.
- M₂ acts like a current source to the rest of the circuit.

Small-Signal Resistance of I-Source

Goal: increase \( r_{oc} \).
Approach: look at amplifier output resistance results … to see topologies that boost resistance.

Improved Current Sources

Looks like the output impedance of a common-source amplifier with source degeneration.
Effect of Source Degeneration

Equivalent resistance loading gate is dominated by the diode resistance ... assume this is a small impedance.

Output impedance is boosted by factor \(1 + g_m R_s\).

Cascode (or Stacked) Current Source

Insight: \(V_{DS2} = \text{constant AND } V_{DS2} = \text{constant}\)

Small-Signal Resistance \(r_{oc}\):

\[R_c = (1 + g_m R_s) r_n\]
\[R_c = (1 + g_m r_n) r_n\]
\[R_c = g_m r_n^2 \gg r_n\]

Current Sinks and Sources

Sink: output current goes to ground
Source: output current comes from voltage supply

Drawback of Cascode I-Source

Minimum output voltage to keep both transistors in saturation:

\[V_{OUT, MIN} = V_{GS2, MIN} + V_{DS2, MIN}\]
\[V_{DS2, MIN} > V_{GS2} - V_T = V_{DSAT2}\]
\[V_{D4} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_T\]

\[V_{OUT, MIN} = V_{GS2} + V_{GS4} - V_T\]
Current Mirrors

We only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.

Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination “works”

CS<sub>1</sub>  
\[ A_c = \frac{-g_{m1} \left( r_{m1} \| r_{m2} \right) \times \left( -g_{m2} r_{m2} \right)}{g_{m1} g_{m2} \left( r_{m2} \| r_{m1} \right) \left( r_{m2} \right)} \]

CS<sub>1,2</sub>  
\[ R_{in} = R_{in1}, \quad R_{out} = R_{out2} \]

CS<sub>2</sub>  
\[ A_c = \frac{1}{g_{m1} + g_{m2}} \]

Summary of Cascaded Amplifiers

**General goals:**

1. Boost the gain (except for buffers)
2. Improve frequency response
3. Optimize the input and output resistances:

<table>
<thead>
<tr>
<th></th>
<th>( R_{in} )</th>
<th>( R_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage:</td>
<td>( \infty )</td>
<td>0</td>
</tr>
<tr>
<td>Current:</td>
<td>0</td>
<td>( \infty )</td>
</tr>
<tr>
<td>Transconductance:</td>
<td>( \infty )</td>
<td>( \infty )</td>
</tr>
<tr>
<td>Transresistance:</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Cascading stages

Input resistance: \( \infty \)

Voltage gain (2-port parameter):
\[ A_v = \frac{-g_{m1} \left( r_{m1} \| r_{m2} \right) \times \left( -g_{m2} r_{m2} \right)}{g_{m1} g_{m2} \left( r_{m2} \| r_{m1} \right) \left( r_{m2} \right)} \]

Output resistance:
\[ R_{out} = \frac{1}{g_{m1} + g_{m2}} \]