Lecture 32:

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Context

Today we are going to review some of the building blocks for multi-stage amplifiers, including current sources and cascode connected devices.

We will also look at the general objectives of multi-state amplifier configurations.

Lecture Outline

- Current Mirrors
- An Example Using Cascodes
- Multistage Amps

Reading

- Chapter 9, multi-stage amplifiers
The Integrated “Current Mirror”

- M₁ and M₂ have the same $V_{GS}$.
- If we neglect CLM ($\lambda=0$), then the drain currents are equal.
- Since $\lambda$ is small, the drain currents will be nearly equal even if $V_{OUT}$ is not equal to $V_{GS1}$.
- $I_{REF}$ is “mirrored” into $i_{OUT}$.
- Works for small and large signals.

Small-Signal Resistance of $I$-Source

- $I_{REF}$ is a constant current source.
- $I_{REF}$ is used to bias the rest of the circuit.

Current Mirror as Current Sink

- The output current of M₂ is only weakly dependent on $V_{OUT}$ due to high output resistance of a long channel FET.
- M₂ acts like a current source to the rest of the circuit.

Improved Current Sources

- Goal: increase $r_{oc}$.
- Approach: look at amplifier output resistance results … for topologies that boost resistance.
- $R_{out} >> r_o$.
Effect of Source Degeneration

- Equivalent resistance loading gate is the small signal resistance of the the diode connected FET ... assume this is a small impedance
- Output impedance is boosted by factor \((1 + g_m R_g)\)

Cascode (or Stacked) Current Source

Insight: \(V_{GS2} = \text{constant AND} \quad V_{DS2} = \text{constant}\)

Small-Signal Resistance \(r_{oc}\):

\[
R_o \approx (1 + g_m R_g) r_e
\]
\[
R_o \approx (1 + g_m r_e) r_e
\]
\[
R_o \approx g_m r_e^2 \gg r_e
\]

The Cascode Configuration

Common source / common gate cascade is called a cascode

Remember that the common gate amplifier can take a poor current source and turn it into a better one.

Drawback of Cascode I-Source

Minimum output voltage to keep both transistors in saturation:

\[
V_{OUT,MIN} = V_{DS4,MIN} + V_{GS2,MIN}
\]
\[
V_{GS2,MIN} > V_{GS2} - V_T \Rightarrow V_{GS2} = V_{GSAT2}
\]
\[
V_{G4} > V_{GSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_T
\]
\[
V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_T
\]
**Current Sinks and Sources**

*Sink:* output current goes to ground  

*Source:* output current comes from voltage supply

**Multistage Amplifiers**

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD and the npn versions of CE, CB, and CC (for a BiCMOS process)

What are the constraints?

1. Input/output resistance matching
2. DC coupling (no passive elements to block the signal)

**Current Mirrors**

We only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.

**Summary of Cascaded Amplifiers**

*General goals:*

1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$R_{in}$</th>
<th>$R_{out}$</th>
</tr>
</thead>
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<tr>
<td>Voltage</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Current</td>
<td>0</td>
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</tr>
<tr>
<td>Transconductance</td>
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<td>$\infty$</td>
</tr>
<tr>
<td>Transresistance</td>
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<td>0</td>
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</table>
Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination “works”

Results of new 2-port: \( R_{in} = R_{in1}, R_{out} = R_{out2} \)
\[
A_v = -G_m \left( R_{in2} \parallel R_{out2} \right) \times \left( -G_m R_{out2} \right)
\]
\[
A_v = G_m G_{n2} \left( R_{in2} \parallel R_{out2} \right) \left( R_{out2} \right)
\]

Add a Third Stage: CC

Goal: reduce the output resistance
(important spec. for a voltage amp)

Output resistance:
\[
R_{out} = \frac{1}{g_{m3}} \beta + \frac{R_s}{g_{m3}} + \frac{r_{eb2}}{\beta}
\]

Using CMOS Stages

Input resistance: \( \infty \)

Voltage gain (2-port parameter): \( A_v = -g_{m1} \left( r_{in1} \parallel r_{out1} \right) \times g_{m2} \left( -r_{o2} \parallel r_{o2} \right) \)

Output resistance:
\[
R_{out} = \frac{1}{g_m + g_{nb}}
\]

Multistage Current Buffers

Are two cascaded common-base stages better than one?

Input resistance: \( R_{in} = R_{in1} \)
Two-Port Models

Output impedance of stage #1 (large)

\[ R_{out} = R_{out2} \approx r_{o2} \left( 1 + g_{m2} \beta r_{o2} \right) || r_{oc2} \]

Common-Gate 2nd Stage

\[ R_{out} = R_{out2} \approx r_{o2} \left( 1 + g_{m2} r_{o2} \right) || r_{oc2} \]

Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available
Output of one stage is directly connected to the input of the next stage → must consider DC levels ... why?

Alternative CG-CC Cascade

Use a PMOS CD Stage: DC level shifts upward
CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case:
\[ I_{BLAS2} = 0 \text{ A} \]

CG Cascade: Sharing a Supply

First stage has no current supply of its own \( \Rightarrow \) its output resistance is modified

The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own

Cascode Two-Port Model

Output resistance of first stage

\[ R_{out,CS} = R_{down,CS} = r_{o1} \]

\[ R_{out} \parallel r_{o2} \parallel (1 + g_{m2}r_{o1}) r_{o2} \]

\[ G_m = r_{o2} \]

\[ R_m = \infty \]

Why is the cascode such an important configuration?
Miller Capacitance of Input Stage

Find the Miller capacitance for $C_{gd1}$

Input resistance to common-gate second stage is low $\Rightarrow$ gain across $C_{gd1}$ is small.