Abstract
Circuit design will be challenging in the future. Meeting high-speed performance requirement while dissipating low energy cannot be accomplished easily. The ability to identify the energy-delay trade-off during the initial design process allows designers to optimize the overall circuit performance. Using an inverter chain as a representative logic element, this paper investigates the energy-delay trade-off issues associated with transistor sizing, supply voltage scaling and $V_T$ adjustment. In addition to these, their combined effects will be studied as well. The paper then concludes with numerous energy-delay trade-off options that can be undertaken in the design process.

Introduction
As the technology continues to advance, following Moore’s prediction, the smallest feature that can be transferred onto the wafer has spectacularly been reduced over the past years. The number of transistors that can be packed in a single die has therefore increased dramatically. While this scaling trend has brought several advantages in terms of improvement in circuit performance and cost, new challenges are being encountered and brought to the community’s attention in the recent years, many begin to question the possibility of the continuation of this scaling trend.

One of the most noticing challenges today is the overheating problem due to the growing power density in a chip. The following plot (Figure 1A) shows the projected $I_{DSAT}$-$V_{DD}$ product vs. year, by adopting the equation below as the power measurement benchmark.

$$\sum I_{DSAT} \times V_{DD} = \text{Estimated Transistor Count} \times \frac{I_{DSAT} \times V_{DD}}{\text{T Tranisistor}}$$

The curve shown below is generated using the data obtained from ITRS 2003.

![Figure 1A – Power aggressiveness of technology](image)

While higher circuit speed is unquestionably pleasant, an increase in the power dissipation is detrimental. It is therefore in all likelihood, that the high power density will eventually place an upper limit on the number of functionalities that can be implemented in a given chip. This would then modify the way in which circuits will be designed. Circuit designers will then have to accommodate to this growing power trend and be forced to become more “energy-conscious” while they attempt to increase the circuit speed, rather than focusing their attentions solely on minimizing the delay of the circuits.

Various methods have been proposed in the past to lower energy consumption. Reducing the supply voltage has been one of the most popular methods being employed. Since $E_{DYN} = C_L V_{DD}^2$, a quadratic reduction in energy can be achieved. A few other techniques are preferred sometimes; these include transistor sizing and $V_T$ adjustment [2]. However, the impact of these energy reduction schemes on circuit performance (namely speed) needs to be addressed at the same time as well. Generally speaking, lowering energy consumption leads to an increase in the delay of a circuit. Properly balancing the energy consumption and delay would lead to the most optimum circuit performance. Therefore, it is critical to identify this energy-delay trade-off early in the design process. Numerous schemes are developed in this paper to investigate this trade-off. These schemes should provide a practical guideline to the designers in designing energy-delay efficient circuits that will meet the challenges of tomorrow.

Static and dynamic energy-delay trade-off due to adjustment of $V_{DD}$ and $V_T$
As mentioned in the previous paragraph, adjusting $V_{DD}$ and $V_T$ is an effective means to reduce energy consumption. The energy-delay trade-off associated with this method will be identified. An inverter chain chosen as the representative circuit element to be studied is shown below.
Figure 2A and 2B show the HSPICE simulation for normalized delay vs. threshold voltage, and leakage power (I_{LEAK}\times V_{DD}) vs. threshold voltage for two values of V_{DD}'s, 1.0V and 1.2V respectively.

Suppose that the original design uses the following combination of supply and threshold voltage, (V_{DD}=1.0V, V_{TH}=0.559V), this operating point corresponds to a normalized delay of 10.3246 units (see blue line, Figure 2A) through the inverter chain. The goal however, is to reduce the normalized delay down to 5 time units. There are two possibilities. In the first design option, one can move down along the blue line, which corresponds to V_{DD}=1.0V, by effectively decreases the threshold voltage until the delay meets the specification. The second possibility is to keep the threshold voltage constant (traveling vertically downwards) and move to a different supply voltage curve, namely the pink curve, which corresponds to V_{DD}=1.2V. The energy-delay trade-off associated with each of the schemes discussed above is summarized in the following table.

In the first energy-delay trade-off option, the threshold voltage is adjusted until the specification (normalized delay = 5) is met. An increase in the static energy consumption is observed. In the second case, V_{DD} up scaling is the utilized technique to reduce delay. The trade-off in the energy in this case is mainly dynamic. Though a small amount of an increase in leakage current should be observed, this component is assumed small. Figure 2B confirms this.

In this section, two design options involving the trade-off between delay and static energy, as well as the delay and the dynamic energy are presented. Depending on the specific application, one trade-off option might be preferred over the other. For instance, if a logic circuit is known beforehand that it would be mostly idle during operation, minimizing the static dissipation caused by the leakage current should be the primary objective. Therefore, the second design option involving the V_{DD} adjustment would be favored in this case.

**Energy-delay trade-off due to transistor sizing**

Transistor sizing is an effective method to improve performance, both speed and energy. Consider once again the inverter chain used previously. This will be again the circuit element to be studied this section.

To achieve minimum delay through the chain, prior work [3] has shown that the optimum fan-out of each stage should be sized to be equal to the geometric mean of the fan-outs of its neighbors. However, this sizing technique does not take into account of the energy consumption of the chain. Consequently, the energy consumption of the entire structure is not optimized. Therefore, in order to fully optimize circuit performance (speed and energy in particular), appropriately balancing the trade-off involving energy and delay is critical. To further illustrate this idea, the following design example is presented. The goal of this example attempts to answer the following question: What is the maximum energy saving that can be achieved relative to the energy dissipation of the buffer chain that produces minimum delay, if the propagation delay is allowed to increase by 10%?

**Design Example**

From [3], the minimum delay through the chain is achieved when the fan-out of each stage is sized so that (Here, I will assume that the load capacitor C_{l}=128C_{g1}).

\[
 f = \frac{C_{g2}}{C_{g1}} = \frac{C_{g3}}{C_{g2}} = \frac{C_{g4}}{C_{g3}} = \frac{C_{g5}}{C_{g4}} = \frac{128C_{g1}}{C_{g5}}
\]

Therefore, the minimum delay through the chain is,

\[
 t_{P,MINIMUM\,\,DELAY} = \sum t_{P,i}(1 + f)\]

Since the design specification allows the propagation delay to be increased by 10%, the delay constraint can now be expressed as the following (next page):
The optimum set of \{f_1, f_2, f_3, f_4, f_5\} can be found using the Lagrange Multiplier Method. A well-known technique serves as the constraint and forms the convex programming problem, in which each of the new fan-outs is no longer required to be equal to the geometric mean of the fan-outs of its neighbors.

The dynamic energy dissipation of the buffer chain is:

\[
E = V_{DD}^2 \times \text{Total capacitances in the buffer chain}
\]

\[
= V_{DD}^2 (\gamma C_{g1} + C_{g2} + \gamma C_{g3} + C_{g4} + \gamma C_{g4} + C_{g5} + 128 C_{g1})
\]

\[
= V_{DD}^2 (\gamma - \frac{1}{128} f_1 f_2 f_3 f_4 f_5 + f_1 + \gamma f_1 f_2 + \gamma f_1 f_3 + f_1 f_2 f_3 + f_1 f_2 f_4 + f_1 f_2 f_5 + f_1 f_3 f_4 + f_1 f_3 f_5 + f_2 f_3 f_4 + f_2 f_3 f_5 + f_2 f_4 f_5 + f_3 f_4 f_5) \quad < \text{Equation 2}
\]

Combining <Equation 1> and <Equation 2> together forms the convex programming problem, in which <Equation 1> serves as the constraint and <Equation 2> is the function to be minimized. A well-known technique known as the Lagrange Multiplier Method can be used to find the optimum set of \{f_1, f_2, f_3, f_4, f_5\}. The solution returns the minimum achievable energy dissipation.

Applying the optimization concept described above, the maximum energy reduction attainable is calculated for the delay increase varying from 1% to 40%. The plot (Figure 3) below shows the simulation result (0.18\mu m TSMC CMOS technology model files are used, and 8 is found from HSPICE simulation to be approximately 1.27646. The power supply voltage assumed here is 1.8V).

![Energy & Area Reduction - By Tuning Vdd and Transistor Sizes](image)

**Figure 3** – Reducing energy consumption by trading off delay

To conclude this design example, from the graph above (green line), by tolerating a 10% increase in delay, 34.2587% decrease in energy dissipation can be achieved.

Simultaneously scaling V_{DD} and sizing transistors to achieve the best energy reduction.

Furthermore, an additional benefit gained from trading off delay to lower the energy consumption is the decrease in the overall area of the circuit. The pink line in Figure 3 shows the reduction in area for this particular inverter-chain example, the area saving is as high as 60%. In summary, if we can afford to reduce circuit speed by some tolerated margin, the advantages gained are twofold – dramatic energy and area reductions.

**Energy-delay trade-off due to insertion of interconnect structure**

In this section, I plan to study the effects of inserting interconnect structure into logic circuits. I hope to demonstrate that by properly sizing transistors, placing buffers in the suitable locations, and by carefully evaluating the energy-delay trade-offs, maximum gain in performance in terms of energy and speed can be achieved. Past activity found in Rabaey’s textbook [4] has shown a simple case in which it consists of a buffer chain with inserted interconnect elements, an example is given that allows one to calculate the optimum sizing of the transistors that would lead to the minimum delay. I plan to take this subject to the next level and discuss the effect that this sizing technique has on the overall energy consumption of the structure.

**Conclusion**

In this midterm report, energy-delay trade-off issues that frequently occur in the design of digital circuits are identified and examined. An inverter chain is used as the logic element to be studied throughout this work. It is discovered that by properly balancing the energy consumption and delay, maximum benefits in terms of the speed, energy (and even area) can be derived.

**Bibliography**


