Lecture 34

- Last time:
  - Improved current sources and current mirrors
  - Start multistage amplifiers
- Today:
  - More examples of cascades
  - DC coupling issues

Improved Current Sources

Goal: increase $r_{oc}$
Approach: look at amplifier (?) output resistance results
... to see topologies that boost resistance
Cascode (or Stacked) Current Source

Insight: $V_{GS2} = \text{constant AND}$ $V_{DS2} = \text{constant}$

Small-Signal Resistance $r_{oc}$:

$$h_{21} = \frac{Z_{in}}{Z_{out}}$$

$Z_{in}$ = $\text{constant}$

$Z_{out}$ = $\text{load}$

$Z_{in}$ = $\text{resistor}$

$Z_{out}$ = $\text{load}$

Dept. of EECS

University of California at Berkeley
Current Sinks and Sources

Sink: output current goes to ground

Source: output current comes from voltage supply

\( I_{REF} \)

\( V_{DD} \)

\( V_{OUT} \)

\( R_{out} = 10 \Omega \)

P.MOS

N.MOS

\( V_{DD} \)

\( V_{OUT} \)

\( V_{REF} \)

\( M_1 \)

\( M_2 \)
Drawback of Cascode I-Source

Minimum output voltage for all transistors saturated:

\[ V_{\text{OUT}, \text{MIN}} = V_{DS4, \text{SAT}} + V_{s4} = V_{DS4, \text{SAT}} + V_{GS2} \]
Multistage Amplifiers

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD and the
npn versions of CE, CB, and CC (for a BiCMOS process)

What are the constraints?

1. Input/output resistance matching

2. DC coupling (no passive elements to block the signal)