1) Examine the figure below (please pay special attention to large signal nomenclature: total signal is lower case with upper case subscript. Large signal is upper case with upper case subscript and small signal is small case with small case subscript):

- **a)** Assume that the voltage total signal source is \( V_S(t) = 3V \cos(2\pi \times 100 \text{Hz} \times t) \) and determine the value of \( R \) such that total signal \( V_D \) is limited to 0.8V during forward bias. Assume \( V_{th} = 26 \text{mV} \) and \( I_0 = 10^{-16} \text{A} \). (note that the frequency is so low that any capacitive effects of the pn junction can be neglected.)
- **b)** Draw \( V_D(t) \) and \( V_S(t) \) versus time on the same graph for 2 periods.
- **c)** Replace the source with a large signal / small signal combination of \( V_S(t) = 3V \) and \( v_s(t) = 1mV \cos(\omega t) \). Draw the small signal equivalent circuit and calculate the values of its components. Use the value of \( R \) found in part (a). Neglect the junction capacitance, but calculate the diffusion capacitance assuming that \( \tau_t = 1\mu\text{S} \).
- **d)** An EE105 student claims that at high frequencies, \( V_D(t) \) is zero. Is this possible, and why?
- **e)** If the diode can typically ‘turn on’ in forward bias and have significant currents in only one direction, why do we have devices in our small signal model that allow current in both directions? (For example, during the negative phase of the small signal, small signal current actually flows up in the small signal equivalent circuit.)

2) Given the figure below. You may assume that \( \gamma = 0, \lambda = 0 \), \( W/L = 10 \), \( K_n = 100\mu\text{A/V}^2 \), \( V_{tn} = 1\text{V} \). Both transistors are nmos and the bulk (for both) is tied to ground.
a) Find $V_{out}$

b) If $\gamma$ is not equal to zero, what happens to the value of $V_{out}$ (gets higher, lower, stays the same) and why?