Lecture 36

- Last time:
  - Cascode amplifiers, totem pole voltage supplies
  - Start: two-stage CMOS transconductance amp

- Today:
  - Complete “lecture design” of two-stage CMOS transconductance amplifier

3 Examples

- PS DUE AT 4PM TODAY
- PS 12 OUT FRIDAY
- OH 5/10 TUES 9-11:00
Two-Port Model with Capacitors

Miller capacitance:

\[ C_M = (1 - A_{vc1}) C_{gs1} \]

\[ (-A_{vc1}) C_{gs1} \]

\[ \text{Av}_{	ext{cgh}} = -\frac{g_m}{g_{m2}} \]
Multistage Amplifier Design Examples

Start with basic two-stage transconductance amplifier:

\[ \text{CS (PMOS)} \]

\[ \text{CS (NMOS)} \]

Why do this combination? Teach EE 105! 1st step in multistage design.

\[ \text{DC level shifting?} \]

\[ \text{CS - CS} \]
Two-Stage Amplifier Topology.

Direct DC connection: use NMOS then PMOS

\[ V^+ = +2.5 \text{ V} \]

\[ V^- = -2.5 \text{ V} \]

- Source
- \( V_{\text{BIAS}} \)
- Load
- \( R_{\text{out}} \)
- \( i_{\text{SUP1}} \)
- \( i_{\text{SUP2}} \)
- \( i_{\text{out}} \)
- \( M_1 \)
- \( M_2 \)
- \( R_s \)
- \( R_l \)

Now fill in I-supplies. More like trans-conductance than voltage.

\( \uparrow \)

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Current Supply Design

Assume that the reference is a “sink” set by a resistor.

Must mirror the reference current and generate a sink for $i_{SCF}$.
Simple

Use Basic Current Supplies

$V^+ = +2.5\, \text{V}$

$V^- = -2.5\, \text{V}$

$M_3$, $M_4$, $M_5$, $M_6$, $M_7$

$I_{REF}$, $R_{REF}$

$i_{SUP1}$, $i_{SUP2}$

$I_{D5}$, $I_{D7}$

NOTE: 5 MOSFETS, 1 RESISTOR $\equiv$ 2 "GRAY CIRCLES" I SUPPLIES.
DC Bias: Find Operating Points

※ Find $V_{BIAS}$ such that $V_{OUT} = 0$ V 

Device parameters:

\[
\begin{align*}
\mu_n C_{ox} &= 50 \, \mu A/V^2 \\
V_{Tn} &= 1 \, \text{V} \\
\lambda_n &= 0.05 \, \text{V}^{-1}
\end{align*}
\]

\[
\begin{align*}
\mu_p C_{ox} &= 25 \, \mu A/V^2 \\
V_{Tp} &= -1 \, \text{V} \\
\lambda_p &= 0.05 \, \text{V}^{-1}
\end{align*}
\]

※ Device dimensions (for “lecture” design):

\[
(\frac{W}{L})_n = \frac{50}{2} \\
(\frac{W}{L})_p = \frac{80}{2}
\]

\[
\frac{\mu_p}{\mu_n} = \frac{1}{2}
\]

NEGLECT $2^3$, APPROX. ... Pspice.

HIGHLY CONSTRAIN ... SO MATH WORKS.
Finding $R_{REF}$

Require $I_{REF} = -I_{D3} = 50 \mu A$

$$V^+ = 2.5V$$

$$V_{SG3} = -V_{Tn} + \sqrt{\frac{2I_{D3}}{\mu p C_{ox}(W/L)_{32}}}$$

$$V_{REF} = \frac{5}{50 \mu A} = 100 k\Omega$$

$$R_{REF} = 7.5 - \frac{2.5V}{(1.32V)} = (3.35)$$

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Complete Amplifier Topology

What's missing? The device dimensions and the bias voltage and reference resistor
Small-Signal Device Parameters

Transistors $M_1$ and $M_2$

\[
\begin{align*}
g_{m1} &= 350 \, \mu\text{S} \\
r_{o1} &= 400 \, \text{k}\Omega \\
g_{m2} &= 315 \, \mu\text{S} \\
r_{o2} &= 400 \, \text{k}\Omega
\end{align*}
\]

Current supplies $i_{SUP1}$ and $i_{SUP2}$

\[
\begin{align*}
r_{oc1} &= r_{o4} = 400 \, \text{k}\Omega \\
r_{oc2} &= r_{o6} = 400 \, \text{k}\Omega
\end{align*}
\]
DC Operating Point

$V_{OUT} = 0$
$I_{OUT} = 0$

$V^+ = +2.5 \text{ V}$
$V^- = -2.5 \text{ V}$

$I_{REF} = 50 \mu\text{A}$

$V_{BIAS} = \ldots$

$$I_{D1} = \frac{1}{2} I_{SUP} = 50 \mu\text{A}$$

$sources$ for $PSPICE$

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Two-Port Model

\[ G_{m1} = 0.35 \text{mS; } R_{out1} = 200 \Omega \]

\[ R_{out} = \text{R}_{\text{out1}} = \text{R}_{\text{out2}} = 200 \Omega \]

\[ \text{Find } G_m = \frac{i_{\text{out}}}{v_{\text{in}}} = -G_{m1} \cdot R_{\text{out1}} = -G_{m2} \cdot R_{\text{out2}} = -G_{m1} \cdot R_{\text{out}} = -G_{m2} \cdot R_{\text{out}} \]

\[ v_{\text{in}} = -G_{m1} \cdot R_{\text{out1}} \cdot v_{\text{in}} \]

\[ i_{\text{out}} = G_{m2} \cdot R_{\text{out2}} \cdot v_{\text{in}} \]