Lecture 34

• Last time: Improved current sources and current mirrors

• Today: (CHAPTER 5.1)

– Start multistage amplifiers

– More examples of cascades

– DC coupling issues
Drawback of Cascode I-Source

Minimum output voltage for all transistors saturated:

\[ V_{OUT,MIN} = V_{DS4,SAT} + V_{S4} = V_{DS4,SAT} + V_{GS1} \]

\[ V_{S4} = V_{GS1} + V_{GS2} - V_{DS4} = \sqrt{V^+} \]

\[ V_{OUT,MIN} = V_{GS1} + \sqrt{V^+} \]

\[ V_{OC} = V_{OC}(1 + \frac{g_{ms}R_F}{R_2}) = \frac{V_{OC}}{1 + \frac{g_{ms}R_2}{R_F}} \]
Current Sinks and Sources

Sink: output current goes to ground
Source: output current comes from voltage supply
Current Mirrors

Idea: we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.

\[ V_{DD} \]

\[ +V_{REF} \]

\[ -V_{REF} \]

\[ I_{REF} \]

\[ 10\mu A \]

\[ (\frac{1}{3}) \]
Multistage Amplifiers

Necessary to meet typical specifications for any of the 4 types CE, CS ... GAIN ... NOT ENOUGH. \( R_i \), \( R_o \) aren't that great.

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD and the npn versions of CE, CB, and CC (for a BiCMOS process)

What are the constraints?

1. Input/output resistance matching... GOALS IN CHAPTER 8.

2. DC coupling (no passive elements to block the signal)
Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination "works"

Results: \( R_{in} = R_{in1}, \quad R_{out} = R_{out2}, \quad A_v = \frac{V_{out}}{V_{in}} = \frac{R_{out}}{R_{in}} \)

\( R_{in} = R_{in1} \)

\( R_{out} = \frac{V_{out}}{I} \)

\( R_{out} = \frac{V_{out}}{I} \) (Remember, \( R_{s} \) then cut)
Add a Third Stage: CC

Goal: reduce the output resistance
(important spec. for a voltage amp)

Output resistance:

\[ R_{out} = \left( \frac{1}{g_{m3}} \right) + \frac{R_{S3}}{B_0} \]

\[ = \left( \frac{1}{g_{m3}} \right) + \frac{R_{S3}}{B_0} \]

User: *LARGE LOAD* Too SMALL Rin

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