Lecture 34 (B)

Last time:
- Cascade
- Multi-stage (Ch. 3)

Today:
- 2-port models
  - Not basic compact
  - 4-27 models
- More examples:... current buffer
- DC coupling

- Issue size larger
- Source
- Common
- BJT stages
- BJT stages
- MOS stages
- 3G
- 3
Using CMOS Stages:

Input resistance: $R_{in} = R_{in} = 0$

Voltage gain (2-port parameter): $A_{in} = R_{in}$

Output resistance:

Why have CMOS? We will use FET in better ways.

For $CE$, $CE_L$
Multistage Current Buffers

Are two cascaded common-base stages better than one?

Input resistance: \( R_{in} = R_{in1} \frac{R_{in} + R_{out}}{R_{in} + R_{out} + R_{in2}} \)
Two-Port Models

\[ R_{out2} \equiv r_{02}(1 + g_{m2}r_{\pi2}) \parallel R_{s2} \]

\[ R_{out} = R_{out2} + \frac{r_{oc2}}{R_{s2}} \]

Replace \( R_{s2} \) with CB1

\[ R_{s2} = R_{out1} \parallel \frac{1}{g_{m2}r_{\pi2}} \]

\[ R_{s2} = R_{oc2} \parallel \frac{1}{g_{m2}r_{\pi2}} \]

NOT \( R_{s2} \) is not equivalent to \( R_{s1} \)
Common-Gate 2\textsuperscript{nd} Stage

\[ R_{out} = R_{out2} \approx r_{02} \left(1 + g_{m2} R_{S2}\right) \parallel r_{oc2} \]

\[ R_{S2} = \frac{R_{out1}}\]
## Summary of Cascaded Amplifiers

**General goals:**

1. **Boost the gain parameter** (except for buffers)
2. **Optimize the input and output resistances**

   **CHAPTER 8, SEC. 1**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$R_{in}$</th>
<th>$R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Current</td>
<td>0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transconductance</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transresistance</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available

Output of one stage is directly connected to the input of the next stage → must consider DC levels ... why?

\[ V_{BE} = 0.7V \]

\[ I_E \times R_A. \]

\[ V = 3.2V \]

\[ V_{CE} \]

\[ V_{PS} \]

\[ V_{GS} = 1.5V \]

\[ V_{DS} = 5.0V \]

\[ V_{DD} = 5.0V \]

\[ 2.5V \]

\[ 0V \]

\[ Isup_1 \]

\[ Isup_2 \]

\[ 100mA \]

\[ 1mA \]
Alternative CG-CC Cascade

Use a PMOS CD Stage: DC level shifts upward

\[ V_{SS} = 1.5 \text{ V} \]

\[ V_{SS} = -V_{T} + \frac{2 (1 - \epsilon) V_{D} (V_{DD} - V_{T})}{V_{DD}} \]

\[ 0.5 \]

\[ 2.5 \text{ V} \]

\[ 5.0 \text{ V} \]

\[ 1.7 \text{ V} \]

\[ 3.2 - 1.5 \]

\[ \text{CD1} \]

\[ \text{CG2} \]

\[ \text{PMOS Variant} \]

Much better.
CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case:
\[ I_{BIAS2} = 0 \text{ A} \]

Different \( I_D \)’s … some advantage

\[ /\gamma \text{m} \]
• Two-Port Model of Common-Gate Cascade with Shared Current Supply

\[ R_{av1} = R_{down} = (1 + g_m R_s) R_{oc} \]

\[ R_{av} || R_{down} = R_{oc} || (1 + g_m R_s) R_{oc} \]