Lecture 19

- Last time:
  - DC and small-signal model of the forward-biased diode

- Today:
  - the npn bipolar junction transistor (BJT):
    large-signal characteristics

Bipolar Transistor Lab.

Exams: Pick up in 497 Cory from Robin.
Remakes: Drop off in 497 with Robin.

My OH Tues: 10:30-12. G 2-3 PM.

Dept. of EECS

University of California at Berkeley

Read: 99. 391-395 413-416 (Ebers-Moll)
CRUDE DC (LATCHED SIGNAL) MODEL

\[ \begin{align*}
    I_0 &= 0A \\
    V_0 &= 0.2 \text{V} \\
    V_0 &= V_{BB} (-12.5 \text{V}) \quad (100) \\
    V_0 &= 2.2 \text{V} \quad (101) \\
\end{align*} \]

\text{VERTICAL LINE}

\text{LET IT BE THE}

\text{LATCHING POINT}

\text{VERTICAL LINE}

\text{IN}

\text{REF}

\text{OFF}

\text{ON}
Large-Signal Model

- $I_D$ vs $V_D$ graph
- $b (\mu A)$ vs $V_D$ graph
- Measurement point
- Vertical line ($0.7 \text{ V battery}$)
- $I_D = 0.7 \text{ V}$
- $V_{BD}$
- $I_D = 10^{-16} \text{ A}$
- $100 \Omega$
- $I_D = I_0 (e^{V_D/V_T} - 1)$
- $V_T = 0.7 \text{ V}$
- Series resistance
- $\Phi_g = \Phi_b - V_D$
Small-Signal Model: \( r_d \)

Forward-bias assumed \( \rightarrow V_D = 0.7 \) V (approx)

\[
i_D(t) = I_O e^{v_D(t)/V_{th}} - 1 \approx I_O e^{v_D(t)/V_{th}} - 1\]

Substitute \( v_D(t) = V_D + v_c(t) \):

\[
i_D(t) = I_O e^{v_D(t)/V_{th}} - 1\]

Quasi-static

Slope... Conductance

 conductance \( \approx -1 \)

\[
0.7/0.026 = \text{Huge!!}
\]

\[
0.7/0.06 = 10
\]

\[
0.7/0.06 = 10^{-12}
\]
Power Series Expansion

\[ e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots \]

Can quantify the limit of the linear approximation

\[ e^x \approx 1 + (x + 1)(\frac{e}{x+1}) \approx \frac{e}{x+1} \]

\[ \text{error} = \frac{e}{x+1} \]

\[ \text{ratio} = \frac{e}{x+1} \]

\[ \frac{e}{x+1} \approx e \]
Graphical Interpretation

\[ i_D = I_D \left( 1 + \frac{V_D}{V_I} \right) \]

\[ V_D = A V_D \]

\[ \frac{\Delta i_D}{\Delta V_D} = \frac{1}{V_T} = \frac{A \Delta i_D}{\Delta V_D} \]

\[ V_D = V_T \]

**Small Resistor**

Not quite zero.
Physics of Diffusion Capacitance

carrier concentrations (cm⁻³)

metal contact to n region

n-type

p-type

important point... These aberrations
Diffusion Capacitance

Depletion region narrows under forward bias, increasing capacitance to $C_f = 1.4 \cdot C_0$. For $V_b = 0.3 V$.

Dominant capacitance is from storage of minority carriers in the diode's p and n regions: the diffusion capacitance.

$$C_f = \frac{C_r}{V_b - V_r}$$
Diffusion Capacitance

Minority carrier charge storage is proportional to the DC diode current:

\[ C_d \approx \left( \frac{I_D}{V_{th}} \right) \tau_T = g_d \tau_T \]

where \( \tau_T \) is the diode's transit time.

\[ \leq 1 \text{ps} \]

\[ C_d \approx \text{HUGE} \]

But \( C_d \) is big! (relative to \( C_j \))
Bipolar Transistor Structure

- n^+ polycrystalline silicon contact to n^+ emitter region
- p-type base
- n^- p-n sandwich (intrinsic nnp transistor)
- n^+ buried layer
- field oxide
- metal contact to base
- metal contact to collector

Circa 1992: IBM 2 Micron, wax chip
Circa 2000: BJT+ CMOS, IBM only

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nPN Bipolar Transistor Layout

- (base) #2
- (emitter) (TOP)
- edge of n buried layer (collector) #j
- field oxide
- n+ emitter area, $A_E$ (intrinsic nPN transistor)
- p+
- p
- p
- n+
- (collector)
Measuring the BJT's Collector Characteristics

\[ I_C = I_C(I_B, V_{CE}) \]
Collector Characteristics

- $I_C$ (μA)
  - $I_B = 2.5$ μA
  - $I_B = 2$ μA
  - $I_B = 1.5$ μA
  - $I_B = 1$ μA
  - $I_B = 0.5$ μA
  - $I_B = 500$ nA

- $V_{CE}$
  - $V_{CE} = 0.1$ V
  - $V_{CE} = 0.2$ V

- $I_E = 1$ mA
- $I_E = 2$ mA

- (reverse active)

- (saturation) ... MOS TRIDE
- (forward active) ... MOS SAT.