- MOSFET Spice Model
- P-channel MOSFET
- Complete small-signal model: add capacitors

Today:

Last time:

Lecture 16
Putting Together a Circuit Model

\[ \text{gate} \]

\[ v_{gs} \]

\[ v_{ds} \]

\[ i_d = \frac{v_{gs}}{r_0} \]

\[ K_C \]

\[ \text{drain} \]

\[ \text{source} \]

\[ i_{ds} = \frac{\Delta v_{ds}}{\Delta i_d} \]

\[ = \frac{v_{ds}}{i_d} \]

\[ \text{YES!!} \]
\[ \Delta i_0 = \frac{2 i_0}{\Delta V_{ds}} + \frac{2 i_0}{\Delta V_{bs}} \]

Math 53

No DC IN

Source CRT KCL

5.5

\[ g_m = \sqrt{2 \mu_C C_W I_D} \]
Role of the Substrate Potential

- Need not be the source potential, but \( V_B < V_S \)

Effect: changes threshold voltage, which changes the drain current...substrate acts like a "backgate".

\[
\begin{align*}
\frac{\partial i_D}{\partial V_{BS}} &= Q \\
\Delta i_D &= \frac{\Delta V_{BS} Q}{g_{mb}} \\
Q &= (V_{GS}, V_{DS}, V_{BS})
\end{align*}
\]
$I_D = \mu_n C_w (W/2L) (V_{GS} - V_{TH})^2 (1 + \frac{1}{2 \mu_n V_{DS}})$

**Backgate Transconductance**

\[
V_{TH} = V_{TH0} + V_n \left\{ \frac{\sqrt{-V_{GS} - 2Q_n}}{C} \right\}^{e^{(V_{DS})}} - 0.3 \ldots - 0.4
\]

\[
V_{GS}, V_{BS} \quad V_{TH}, V_{BS}
\]

**Result:**

\[
g_{mb} = \left. \frac{\partial i_D}{\partial V_{BS}} \right|_Q = \left. \frac{\partial i_D}{\partial V_{TH}} \right|_Q \left. \frac{\partial V_{TH}}{\partial V_{BS}} \right|_Q \]

\[
= \frac{T_n \cdot T_m}{2 \sqrt{-2Q_n - V_{DS}}} - \frac{T_n}{2 \sqrt{-2R - V_{DS}}}
\]
MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.

$C_{gs} \neq C_{dv}$

Skinny II plate $n^+$ poly/Si/float $n^+$ poly/box Si

Drain $C_{ds} = C_{ov}$

Depletion region voltage

For $V_{ds} \leq V_{th}$ (for saturation, it's for a wedge)

$\frac{288}{V_{ds}}$
Gate-Source Capacitance $C_{gs}$

Wedge-shaped charge in saturation $\Rightarrow$ effective area is $(2/3)WL$

$C_{gs} = (2/3)WL C_{ox} + C_{ov} = \frac{W}{L} C_{ov}$

Overlap capacitance along source edge of gate $\Rightarrow$

$C_{ov} = L D WC_{ox}$

(Underestimate due to fringing fields)
Four-Terminal Small-Signal Model

\[ I_{in} = \frac{1}{2} I_G \]

\[ \frac{Z_{in}}{2} = \frac{1}{2} \frac{G_{mI}}{G_{ds}} \]

\[ V_{gs} = V_{bs} + V_{bs} \]

\[ C_{IN} = f(V_{GS}) \]

\[ \text{Charge} = \frac{C_{IN}}{V_{OLT}} \]
Gate-Drain Capacitance $C_{gd}$

Not due to change in inversion charge in channel

Overlap capacitance $C_{ov}$ between drain and source is $C_{gd}$
Junction Capacitances

Drain and source diffusions have (different) junction capacitances since $V_{SB}$ and $V_{DB} = V_{SB} + V_{DS}$ aren't the same.

Complete model (without interconnects) $g_{th} = 0.1 \Omega$.
P-Channel MOSFET

Measurement of $-I_{Dp}$ versus $V_{SD}$, with $V_{SG}$ as a parameter:

$V_{SG} = V_{DP} - V_{GS}$

Plot $-I_{DP}$ vs. $V_{SG}$, $V_{SD}$ vs. $V_{SG}$

Parameter: $V_{TP} = -1V$.

$-I_{DP} > 0$.
Square-Law PMOS Characteristics

\[ V_{SD} = V_{SG} + V_{TP} = V_{SG} - 1 \text{ V} \]

\[ V_{SG} = 3.5 \text{ V} \]

\[ V_{SG} = 3 \text{ V} \]

\[ V_{SG} = 25 \]

\[ V_{SG} = 0, 0.5, 1 \text{ V} \]

\[ (\text{cutoff region}) \]

\[ V_{SG} = 2 \text{ V} \]

\[ V_{SG} = 1.5 \text{ V} \]

\[ I_{D_{sat}} = \frac{\mu C_{ox}(V_{LS}X)(V_{SG} + V_{T})}{1 + 2V_{SD}} \]

\[ V_{SD} = V_{SS} + V_{T} ; V_{SS} = -V_{DD} \]
Small-Signal PMOS Model

\[ r_0 = \frac{1}{\lambda_p (-D_p)} \]

Small-Signal Model

\[ r_{dl} = \left( \frac{\partial i_d}{\partial v_{ds}} \right) = 0 \]

\[ \theta_{\text{vdd}} = \infty \]

Department of EECS
MOSFET SPICE Model

Many "levels" ... we will use the square-law "Level 1" model
See H&S 4.6 + Spice refs. on reserve for details.

```
.MODEL MODN NMOS LEVEL=1 VTO = 1 KP = 50U LAMEDA = .033 GAMMA = .6 + FHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 1E-4 CJSW = 5E-10 + NJ = 0.5 PB = 0.95

.MODEL MODP PMOS LEVEL = 1 VTO = -1 KP = 25U LAMBDA = .033 GAMMA = .5 + FHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 3E-4 CJSW = 3.5E-10 + NJ = 0.5 PB = 0.95
```