Lecture 35

• Last time:
  – More examples of cascades
  – DC coupling issues

• Today:
  – Cascode amplifiers
  – Totem pole voltage supplies
  – Start: multistage amplifier design examples
The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own
Cascode Two-Port Model

Output resistance of first stage = \( R_{out,CS^*} = R_{down,CS} = r_{o1} \)

Why is the cascode such an important configuration?
Miller Capacitance of Input Stage

Find the Miller capacitance for $C_{gd1}$

Input resistance to common-gate second stage is low $\rightarrow$ gain across $C_{gd1}$ is small.
Two-Port Model with Capacitors

Miller capacitance: \( C_M = (1 - A_vC_{gs1})C_{gs1} \)
Other Cascode Configurations

Basic configuration: transconductance stage followed by current buffer

\[ CE_n-CG_n \quad CS_n-CB \quad CS_p-CG_n \]
Generating Multiple DC Voltages

Stack-up diode-connected MOSFETs or BJTs and run a reference current through them → pick off voltages from gates or bases as references
Multistage Amplifier Design Examples

Start with basic two-stage transconductance amplifier:

Why do this combination?
Two-Stage Amplifier Topology

Direct DC connection: use NMOS then PMOS

\[ V^+ = +2.5 \text{ V} \]

\[ V^- = -2.5 \text{ V} \]
Current Supply Design

Assume that the reference is a “sink” set by a resistor

Must mirror the reference current and generate a sink for $i_{SUP_2}$
Use Basic Current Supplies

$V^+ = +2.5\, \text{V}$

$V^- = -2.5\, \text{V}$

$I_{\text{REF}}$ $R_{\text{REF}}$

$i_{\text{SUP1}}$

$i_{\text{SUP2}}$

$I_{D7}$ $I_{D5}$

$M_3$ $M_4$ $M_5$

$M_6$ $M_7$
Complete Amplifier Topology

What’s missing? The device dimensions and the bias voltage and reference resistor