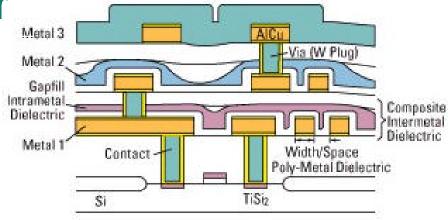
Week 2, Lectures 3-5, February 22-26, 2001

EECS 105 Microelectronics Devices and Circuits, Spring 2001

Andrew R. Neureuther

Topics: Practice Loop and Node Eqns., Two-Ports, Silicon Physics – Carriers, Process Flow and Layout, Sheet Resistance, Squares



Reading for week: (review of EE 40), HS 8.2.2, 9.1, 2.1-2.4, 2.5.4-2.6, 4.1.1, 4.5.7,6.2, 7.1.1,7.7,

Outline: Week 2 Lectures 3-5

L3: More Basic Circuits (HS 8.2.2, 9.1) Loop and Node Equations, Two-Ports

L4: Silicon Physics (HS 2.1-2.4, 2.5.4, 4.1.1, 5.4.7, 6.2, 7.1.1,7.1)

Carriers, Process Flow and Layout

L5: IC Resistors (HS 2.6)

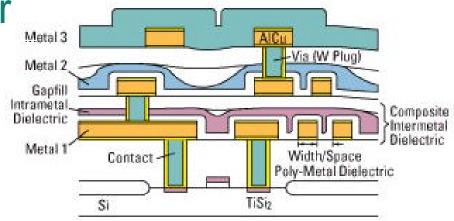
Sheet resistance and Number of Squares

Lecture 3, February 22, 2001

EECS 105 Microelectronics Devices and Circuits, Spring 2001

Andrew R. Neureuther

Topics:
Practice Circuit Analysis,
Two-Ports



Reading: (review of EE 40), HS 8.2.2, 9.1

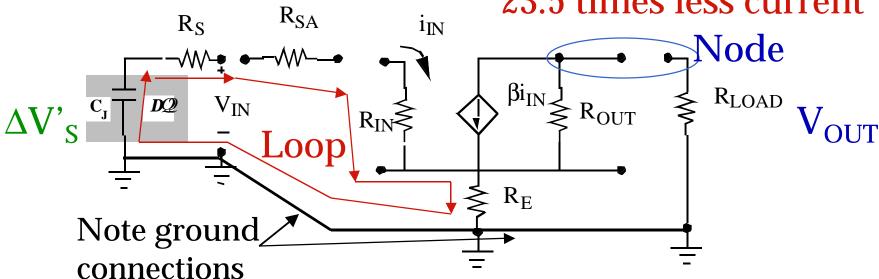
W2 M L3: More Basic Circuits

- Practice circuit analysis
 - R_{IN} with R_{E}
 - » Gain or Rout with R_F
- Standard Two-ports
- Difficulty of two-ports with output coupled back to input

High Input Impedance Circuit



23.5 times less current



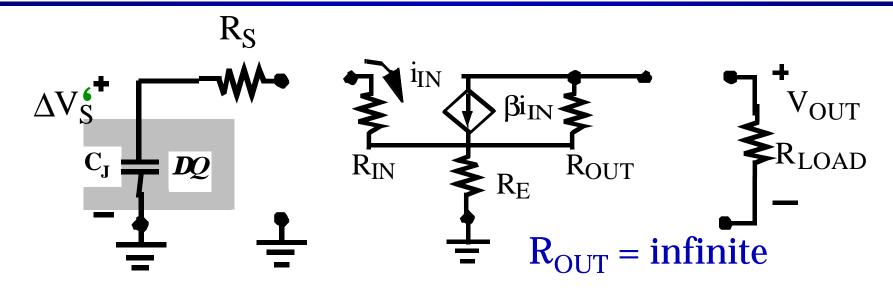
$$V_{OUT} = [\Delta V'_{S}/(R_{S}+R_{SA}+R_{IN EQ})](-\beta)R_{LOAD} = 5 \text{ mV}$$

$$\Sigma V_{i} = 0 => i_{IN}$$
23.5 times smaller gain

Analog Integrated Circuits

Overview and Circuit Value Added

High Input Impedance Circuit

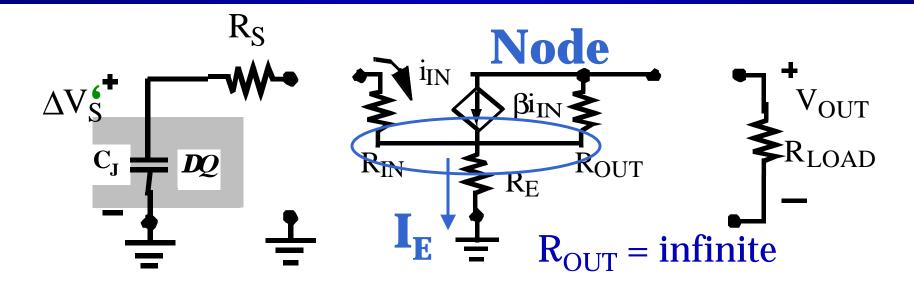


Result:

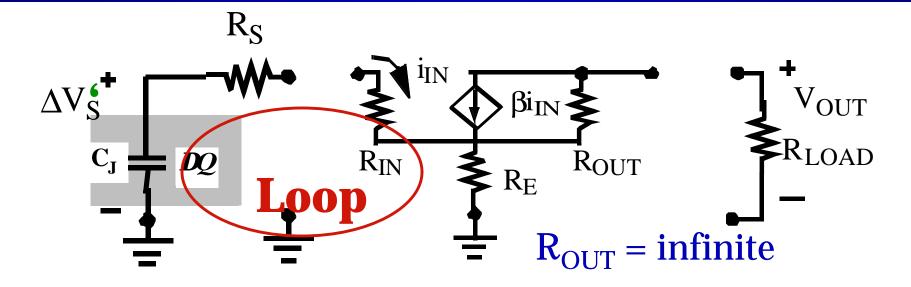
$$\mathbf{V_{OUT}} = [\Delta \mathbf{V'_S}/(\mathbf{R_S} + \mathbf{R_{SA}} + \mathbf{R_{IN EQ}})](-\beta)\mathbf{R_{LOAD}}$$

How is the circuit analysis done?

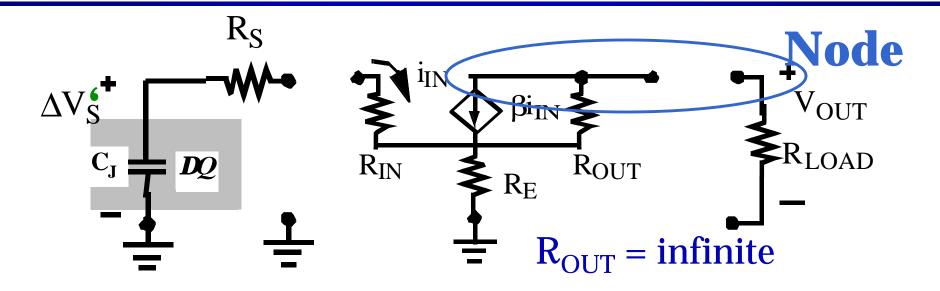
Write a Node Equation for I_E



Write a Loop Equation for I_{IN}

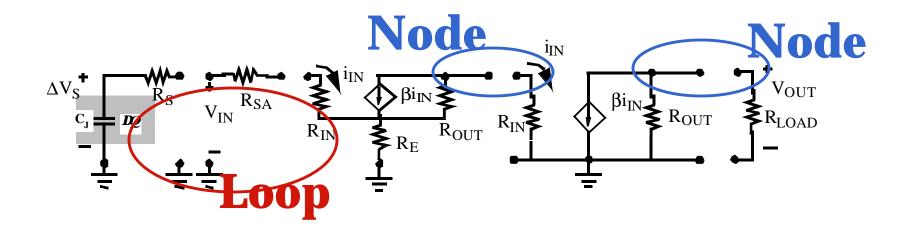


Find $V_{OUT}/\Delta V'_{s}$



$$\mathbf{V_{OUT}}/\Delta \mathbf{V'_S} = [1/(\mathbf{R_S} + \mathbf{R_{SA}} + \mathbf{R_{IN EQ}})](-\beta)\mathbf{R_{LOAD}}$$

Analysis of Multistages

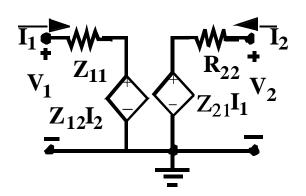


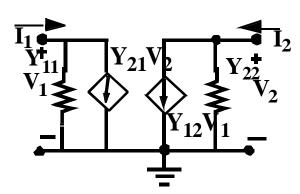
Background on Two-Ports

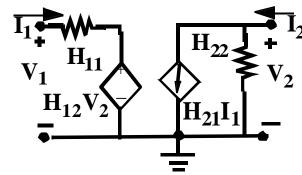
- Designed for cascading components
 - » Hi-Fi components
 - » IC stages of amplifier circuit
- Based on Matrix Multiplication

$$\begin{array}{lll} V_{1} = Z_{11}I_{1} + Z_{12}I_{2} & I_{1} = Y_{11}V_{1} + Y_{12}V_{2} & V_{1} = H_{11}I_{1} + H_{12}V_{2} \\ V_{2} = Z_{21}I_{1} + Z_{22}I_{2} & I_{2} = Y_{21}V_{1} + Y_{22}V_{2} & I_{2} = H_{21}I_{1} + H_{22}V_{2} \\ \hline & Impedance & Admittance & Hybrid_1 \\ & (transresistance) & (transconductance) & (current 1-2) \\ \end{array}$$

Two-Port Equivalent Circuits







$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
 $I_1 = Y_{11}V_1 + Y_{12}V_2$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$
 $I_2 = Y_{21}V_1 + Y_{22}V_2$

$$V_1 = H_{11}I_1 + H_{12}V_2$$

$$I_2 = H_{21}I_1 + H_{22}V_2$$

Two Thevenin

Two Norton

Thevenin input **Norton output**

(transresistance)

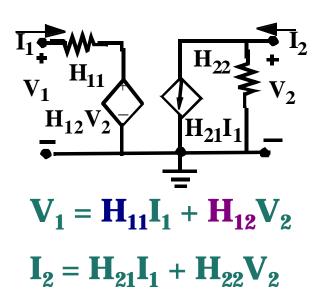
(transconductance)

(current 1-2)

Analog Integrated Circuits

Overview and Circuit Value Added

Finding the Two-Port Parameters

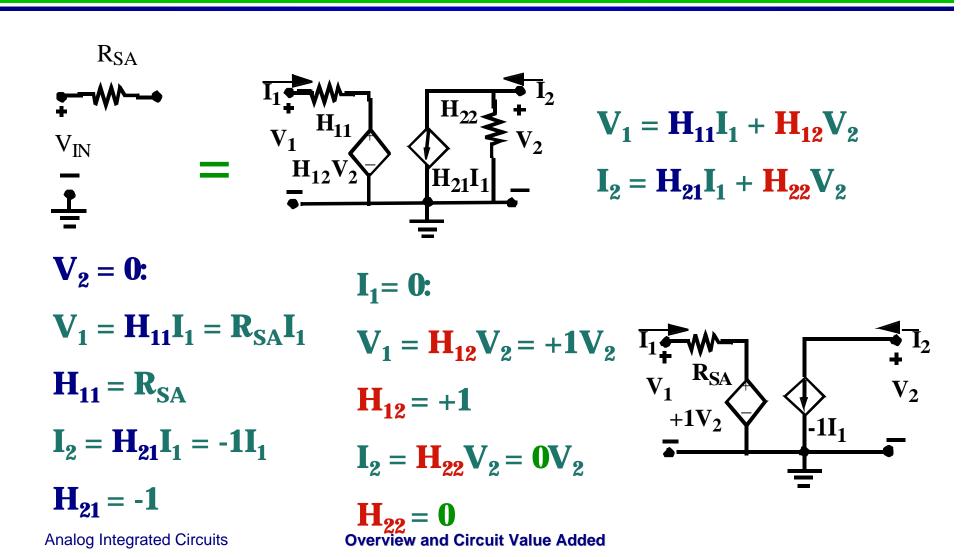


 H_{11} is found by taking V_1 over I_1 when V_2 is zero.

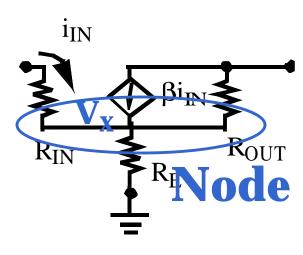
H₁₂ is found by taking V₁ over V₂ when I₁ is zero.

Note: The conditions to determine each matrix element arise from the terminal variables multiplying the right hand side.

Hybrid Two-Port for a Resistor



Find H₁₁ with R_E and R_{OUT}



$$V_1 = \mathbf{H}_{11}\mathbf{I}_1 + \mathbf{H}_{12}\mathbf{V}_2$$
$$\mathbf{I}_2 = \mathbf{H}_{21}\mathbf{I}_1 + \mathbf{H}_{22}\mathbf{V}_2$$

$$V_X = (\beta + 1) i_{IN}/(1/R_S + 1/R_{OUT})$$

$$\mathbf{V_{IN}} = \mathbf{i_{IN}} \; \mathbf{R_{IN}} + \mathbf{V_X}$$

$$\mathbf{H_{11}} = (\mathbf{V_{IN}} / \mathbf{i_{IN}}) |_{\mathbf{V2=0}} =$$

$$R_{IN} + (\beta + 1) (R_S R_{OUT}) / (R_S + R_{OUT})$$

$$V_2 = 0$$
:

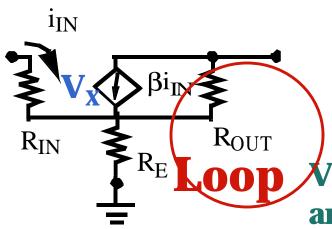
$$R_{OUT}$$
 in $| |$ with R_{E}

Node Eq. For
$$V_X$$

$$i_{IN} - V_X/R_S - V_X/R_{OUT} + \beta i_{IN} = 0$$

Note: R_{IN} depends on R_{OUT} when the output feeds back to the input.

Find H₁₂ with R_E and R_{OUT}



$$V_1 = H_{11}I_1 + H_{12}V_2$$
 $I_2 = H_{21}I_1 + H_{22}V_2$

Voltage V_2 is divided across R_{OUT} and $R_{\rm F}$

$$\mathbf{I_1} = \mathbf{0}:$$

$$i_{IN} = 0$$

$$V_1 = V_X$$

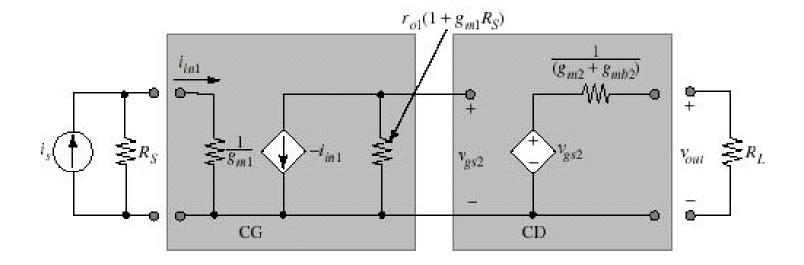
$$\mathbf{V_1} = \mathbf{V_2} \mathbf{R_E} / (\mathbf{R_E} + \mathbf{R_{OUT}})$$

$$\mathbf{H_{12}} = (\mathbf{V_1} / \mathbf{V_2}) \mid_{\mathbf{I1}=\mathbf{0}} = \mathbf{R_E} / (\mathbf{R_E} + \mathbf{R_{OUT}})$$

Note: The voltage source in the input port is not zero when RE is not zero.

Overview and Circuit Value Added

Multistage Amplifiers



This example from the reading in Chapter 8 this week.

Classification of Two-Port Amplifiers

