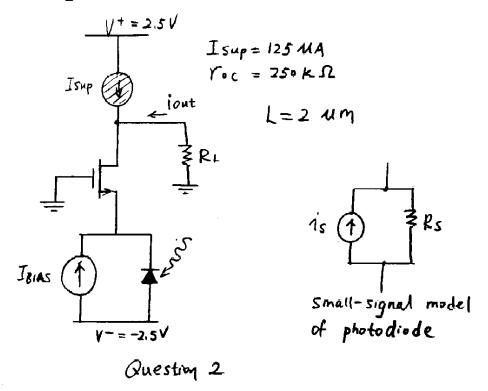
## University of California College of Engineering Department of Electrical Engineering and Computer Sciences

## Problem Set #12 Review Problems - Not Due

EECS105

**FALL, 1998** 

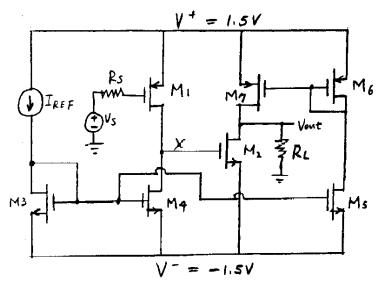
- 1. P8.8
- 2. This circuit buffers the small-signal current from a photodiode. The small-signal model for the photodiode is shown.  $I_{sup} = 125 \,\mu\text{A}$ ,  $r_{oc} = 250 \,\text{k}\Omega$ , and  $L = 2 \,\mu\text{m}$ . Use the MOSFET parameters from p. 319. (Note the typo in the channel length modulation parameters.  $\lambda n = 0.067 \,\text{V}^{-1}$ .)
  - (a) Given that  $I_{out} = 0$  A and  $I_{BIAS} = -125 \,\mu\text{A}$ . Select the width W of the NMOS such that the DC bias on the photodiode is  $V_D = -1.25 \,\text{V}$ .
  - (b) Draw the two-port small-signal model for this amplifier (with source and load).
  - (c) Find the numerical value of the input resistance  $R_{in}$  of this amplifier.
  - (d) Find the numerical value of the output resistance  $R_{out}$  of this amplifier.
  - (e) Find the overall current gain  $i_{out}/i_s$  for this amplifier for the case where  $R_s = 50$  k $\Omega$  and  $R_L = 100$  k $\Omega$ .



4. Default MOS transistor parameters: note that  $\lambda$  depends on L!

NMOS: 
$$\mu_n C_{OX} = 100 \,\mu\text{A/V}^2$$
,  $\lambda_n = [0.1/L] \,\text{V}^{-1} (L \,\text{in } \mu\text{m})$ ,  $V_{Tn} = 1 \,\text{V}$   
PMOS:  $\mu_D C_{OX} = 50 \,\mu\text{A/V}^2$ ,  $\lambda_D = [0.1/L] \,\text{V}^{-1} (L \,\text{in } \mu\text{m})$ ,  $V_{TD} = -1 \,\text{V}$ 

- (a) Determine the width of transistor  $M_1$  in  $\mu$ m so that  $V_x = 0$  V.
- (b) Redraw the circuit with symbolic current supplies replacing the transistor current supplies. Give the numerical value of the DC supply currents; there is no need to calculate the source resistance of this supplies.
- (c) Draw the two-port small-signal model for this two-stage amplifier. There is no need to substitute numerical values for the elements.
- (d) Find the numerical value of the output resistance Rout of this amplifier.
- (e) Find the numerical value of the open-circuit voltage gain  $A_{v}$  of this amplifier in dB.



$$L = 2 \text{ Am for all MOSFET}$$

$$(W/L)_1 = (W/L)_2 = \frac{20 \text{ Am}}{2 \text{ Am}}$$

$$(W/L)_3 = \frac{(0 \text{ Am}}{2 \text{ Am}}$$

$$(W/L)_4 = (W/L)_5 = \frac{20 \text{ am}}{2 \text{ Am}}$$

$$(W/L)_6 = \frac{(0 \text{ am}}{2 \text{ am}}$$

$$I_{REF} = 25 \text{ AA}$$

$$R_S = 5 \text{ K} \Omega$$

$$R_1 = 100 \text{ k} \Omega$$

Question 4

## 5. E5.9

6. An NMOS inverter with current source pull-up shown in the figure has  $(W/L)_n = 6/1.5$  and  $(W/L)_p = 3/6$ ,  $V_{DD} = 3$  V and  $V_B = 0$  V. Use the simplified hand calculation method shown in sections 5.4.1 and 5.4.3. Assume devices are in their constant current region. For this problem, use  $\lambda_n = [0.1/L_n] \text{ V}^{-1} (L_n \text{ in } \mu\text{m})$  and  $\lambda_p = [0.1/L_p] \text{ V}^{-1} (L_p \text{ in } \mu\text{m})$ ;  $\varepsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$ . Refer to p. 319 for other MOS transistor parameters.

(b) Two identical inverters are located 1000  $\mu$ m from the driving inverter. The connecting wire is 2  $\mu$ m wide aluminum and lies on a deposited glass and field oxide layer. The total thickness of the dielectric layer is 1.0  $\mu$ m and you can assume it behaves like a parallel capacitor. The permittivity of the dielectric is  $3.9\epsilon_0$ . Calculate the propagation delay  $t_p$ .

(c) What is the static power consumed by this circuit?

(d) Calculate the device widths such that  $C_{DB} = 100$  fF while maintaining the same  $V_{M}$ .

(e) What is  $t_D$  for the device sizes calculated in (d)?

