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College of Engineering
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Problem Set #11
Due Wednesday, November 11th, 1998

EECS105 **FALL 1998**

Default values to use on this problem set: $V_{Tn} = -V_{Tp} = 1$ V, $V_{DD} = 5$ V, $\mu_N C_{OX} = 50\ \mu A/V^2$, $\mu_P C_{OX} = 25\ \mu A/V^2$, $V_{GS,sat} = 1.5$ V, $V_{CE,sat} = .2$ V, and $V_{BE,sat} = .7$ V

1. Examine the circuit in Figure 1.
   a. What is the circuit's purpose?
   b. What is the minimum v_{OUT} that can be sustained and still have all devices operating in their constant current region?

2. Check out the totem pole in Figure 2. It is decreed that W/L = 10/2 and $I_S = 10^{-15}$ A. You may neglect base current and backgate effect. Assume all devices are operating in their constant-current region.
   a. Solve for V_{OUT1}, V_{OUT2}, and V_{OUT3}.
   b. Maintaining the same V_{OUT1} as part (a), change the W/L of device M_2 so that $V_{OUT2} = 2.4$ V.
   c. How does implementing part (b) change the value of V_{OUT3}

3. Take a good close look at Figure 3. M_R has a device sizing of W/L = 10/2. Assume all devices are operating in the constant current region (surprise!), and neglect backgate effect.
   a. Find $(W/L)_1$ such that $I_{OUT1} = 60\ \mu A$.
   b. Find $(W/L)_2$ such that $I_{OUT2} = 120\ \mu A$.
   c. Find $(W/L)_3$ such that $I_{OUT3} = 300\ \mu A$.

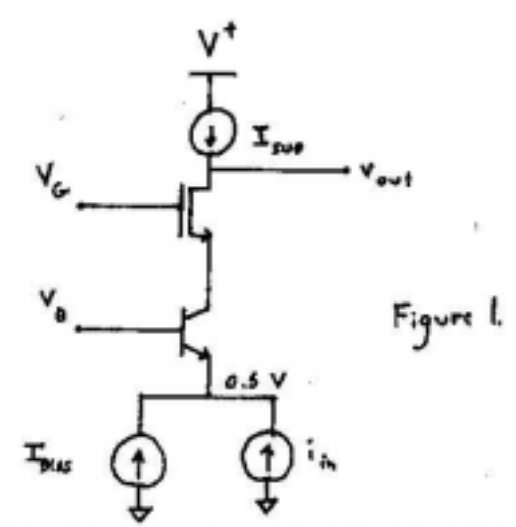

Figure 1.

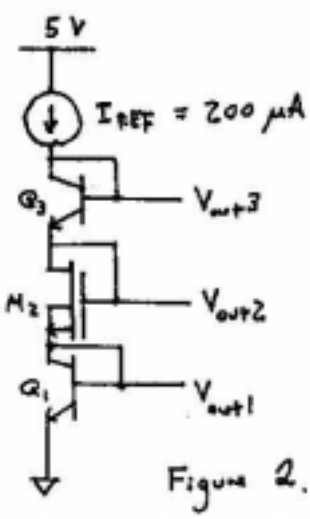

Figure 2.

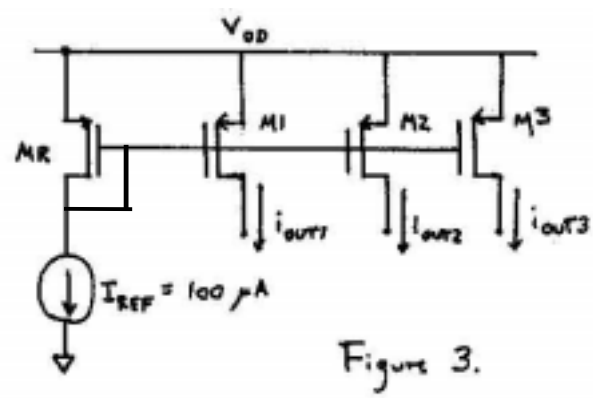

Figure 3.

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4. For the next stage in your education you will compare a bipolar and MOS voltage source. The two sources are shown in Figure 4. I_{REF} = 100 μA, and the device characteristics are as follows:

   BJT Characteristics: $I_S = 10^{-15}$ A, $\beta_F = \beta_0 = 100$, $V_A = 20$ V.

   MOS Characteristics: W/L = 20/2, $V_{Tn} = 0.7$ V, $\lambda_n = 0.03\ V^{-1}$

   a. Find an expression for V_{OUT} as a function of Iout in the bipolar case, and find it's explicit value for Iout = 0. This time do NOT neglect I_B.
   b. Now solve for V_{OUT} in the MOS case.
   c. Solve for the incremental source resistance in the BJT.
   d. Solve for the incremental source resistance in the MOS.

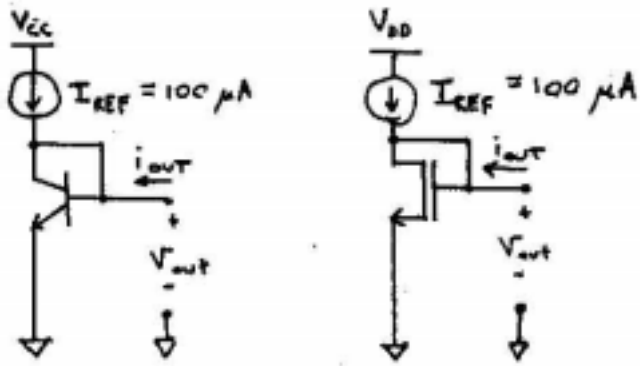

Figure 4.

5. Last but not least, inspect the cascode current source in Figure 5. For the questions, assume that the W/L ratio of all devices is 10 and that I_{OUT} = 100 μA. The PMOS device characteristics are as follows: $V_{Tp} = -0.7$ V and $\lambda_p = 0.03\ V^{-1}$. Assume that all bulk connections are tied to the source.

   a. Calculate the incremental source resistance of the current source.
   b. If I_{OUT} is required to be 20 μA, what is the new W/L of devices M_2 and M_{2B} assuming that I_{REF} remains at 100 μA?
   c. Assuming part (b) is implemented, what is the new incremental source resistance?

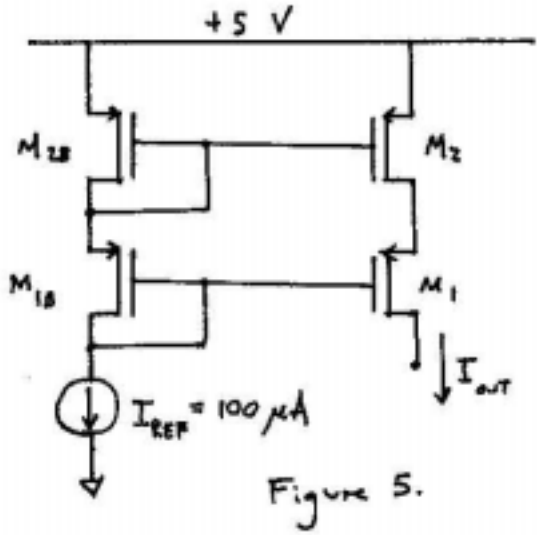

Figure 5.

Notice the new Date and Time for the 2nd Midterm: Friday 6-7:30pm, 20th of November in Sibley
For the latest news, visit our web site: http://www-inst.EECS.Berkeley.EDU/~ee105/
Please post your questions on our newsgroup: ucb.class.ee105
Please return your homework in 558 Cory Hall, to Cheryl Craigwell (cmc@eecs, 642-1237, fax 642-2739), or in class by 11:10am of the due date. Late homeworks will not be graded.