CMOS Static NAND Gate

- Second switching condition: \( V_A = V_{DD} \) and \( V_B \) switches from 0 to \( V_{DD} \)

At \( V_B = V_M \), the current through \( M_1 \) and \( M_2 \) is higher than when \( V_A = V_B \) since the gate voltage on \( M_1 \) is now \( V_{DD} \) and its \( V_{DS1} \) must be smaller \( \rightarrow \) \( V_{GS2} \) is larger. Effective \( k_n \) is increased.

At \( V_B = V_M \), only \( M_4 \) is conducting current \( \rightarrow \) only half the current as for previous switching condition. Effective \( k_p \) is that of device \( M_4 \)

- Result: \( V_M \) is 0.3-0.5 V lower than for \( V_A = V_B \) switching condition, for typical dimensions
NAND Gate Transfer Functions

SPICE is useful to solve for the transfer functions under the various switching conditions (see Ex. 5.7). Note that the backgate effect means that the curves when $V_A$ switches and when $V_B$ switches are not identical.

Results: setting $k_n = 2 k_p$ results in $V_M$ approximately $V_{DD}/2$. 
CMOS NAND Gate Transient Analysis

- Worst-case situation for low-to-high transition: only one of the p-channel transistors is switching (say $M_4$):

$$-I_{Dp} = -I_{D4} = \frac{k_p}{2} (V_{DD} + V_{Tp})^2$$

- For high-to-low transition, consider $M_1$ and $M_2$ in series with effective length at $2L_n$ (worst-case since current is lowest with $V_A = V_B$)

$$I_{Dn} = I_{D_1} = I_{D2} = \mu_n C_{ox} \left[ \frac{W_n}{2(2L_n)} \right] (V_{DD} - V_{Tn})^2 = \frac{k_n}{4} (V_{DD} - V_{Tn})^2$$

- For equal propagation delays, we require $I_{Dn} = -I_{Dp}$

$$\frac{k_n}{4} = \frac{k_p}{2} \rightarrow k_n = 2k_p$$

The factor of 2 mobility difference between the p and n channels indicates that

$$(W/L)_n = (W/L)_p \text{ (2 input NAND gate)}$$

- For an $M$-input NAND gate, we find that

$$(W/L)_n = (M/2) (W/L)_p$$

Note: NOR gates suffer from a factor of $2M$ between the n- and p-channel ratios which makes them unattractive for large fan-in gates
Transistor Sizing (Example)

Logic function $Y = D + [A \cdot (B + C)]$
CMOS Dynamic Logic

- Static NOR gate

![CMOS NOR gate diagram]

Idea: n-channel and p-channel devices separately perform the same logic function.

- replace p-channels with a resistor -->
  \[ Q = \overline{A + B} \]

- replace n-channels with a resistor -->
  \[ Q = \overline{\overline{A} \overline{B}} \]

... two functions are identical by DeMorgan’s Theorem

- Let n-channels perform the logic and get rid of the pull-up devices (or vice versa)
**n-Channel CMOS Dynamic Logic**

- A clock signal $\phi(t)$ charges up load capacitance through $M_P (P = \text{precharge})$ when it transitions from high to low; $M_E (E = \text{evaluate})$ is cutoff and prevents any discharge path of $C_L$ through logic function transistors.

- A clock signal goes high $\rightarrow$ $M_P$ is cutoff, $M_E$ conducts $\rightarrow$ $C_L$ discharges if one of the logic transistors has a high input.

**Payoffs:**

1. large fan-in NOR gates without huge p-channel load devices (also, avoids backgate effect on loads)

2. tends to be fast due to smaller load capacitances

**Drawback:**

1. clock is essential to refresh logic level stored on $C_L$, which complicates the design
n-Channel Dynamic Logic Propagation Delays

Consider “$t_{PLH}$” to be the time required to pre-charge the output node.

Precharge Circuit ($t_{PLH}$)

$V_{DD}$

$M_P$

$V_{OUT}(t = 0) = 0 \text{ V}$

$C_L$

$A$ $B$ $M$ (cutoff)

$n$ Charging current

$$-I_{DP} = \frac{k_p}{2}(V_{DD} + V_{TP})^2$$
n-Channel Dynamic Logic Propagation Delays

Consider “t_{PHL}” to be the worst-case time to evaluate the logical function after clock goes high.

Evaluate Circuit (t_{PHL})
(only one input high)

\[ V_{DD} \]

\[ \phi = 5 \text{ V} \]

\[ MP \text{ (cutoff)} \]

\[ V_{OUT}(t = 0) = 0 \text{ V} \]

\[ CL \]

\[ 5 \text{ V} \]

\[ 0 \text{ V} \]

\[ \ldots \ldots 0 \text{ V} \]

\[ \phi = 5 \text{ V} \]

\[ ME \]

Discharging current: assume \((W/L)_E = (W/L)_A = \ldots (W/L)_M\) and note that the transistors are in series -->effective value is \(k_n / 2\)

\[ I_{D_n} = \mu_n C_{ox} \left( \frac{k_n}{4} \right) (V_{DD} - V_{Tn})^2 \]
Boolean Functions in Dynamic Logic

Examples:

(a) n-channel dynamic logic

\[ Q = (A + B) \overline{C} \]

(b) p-channel dynamic logic

The output is “pre-discharged” to zero by \(M_P\) and is only charged if there is a path through the logic transistors when the clock goes low and \(M_E\) conducts.

\[ Q = \overline{A}B + \overline{C} + \overline{D} \]
CMOS Transmission Gates

- Need: “gate” signals by having a series switch that can be shorted or open-circuited.

- Why n-channel and p-channel in parallel? Only one device (say, n-channel): can’t pass an input voltage \( V_{DD} - V_{Th} \), since device will enter the cutoff region.

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(a) charge-up

(b) discharge
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Pass Transistor Logic

- Advantages: reduced transistor count and higher speed compared with static CMOS
- Disadvantage: reduced noise margins